Problem Solutions

Chapter Eight: NMOS Logic

P8.1. Consider the NMOS gate depicted in Figure 8.30.

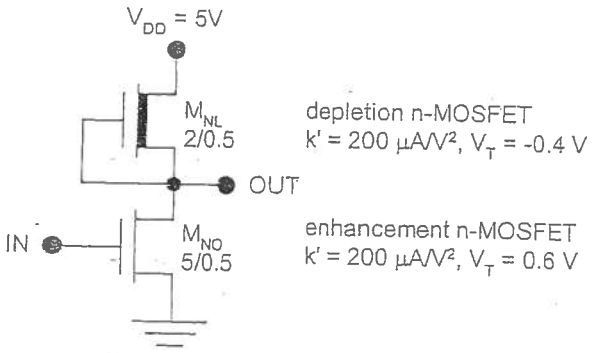

Figure 8.30.

a. Determine V_{IL}, V_{IH}, V_{OL}, and V_{OH}.

b. Determine the noise margins V_{NML} and V_{NMH}.

c. Estimate the average DC dissipation.

Solution.

a. The device transconductance parameters are

$$K_L = \left(\frac{2\mu m}{0.5\mu m}\right) 200\mu A/V^2 = 0.8mA/V^2 \text{ and}$$

$$K_O = \left(\frac{5\mu m}{0.5\mu m}\right) 200\mu A/V^2 = 2.0mA/V^2.$$

The four critical voltages are

$$V_{IL} = V_{TO} + \frac{K_L}{\sqrt{K_O K_L + K_O^2}}|V_{TL}|$$

$$= 0.6V + \frac{2.0mA/V^2}{\sqrt{(2.0mA/V^2)(0.8mA/V^2)+(2.0mA/V)^2}}|-0.4V| = 0.73V$$

,

$$V_{IH} = V_{TO} + 2|V_{TL}|\sqrt{\frac{K_L}{3K_O}} = 0.6V + 2|-0.4V|\sqrt{\frac{0.8mA/V^2}{3(2.0mA/V^2)}} = 0.89V,$$

$$V_{OL} = V_{DD} - V_{TO} \pm \sqrt{(V_{DD}-V_{TO})^2 - \left(\frac{K_L}{K_O}\right)V_{TL}^2}$$

, and

$$= 5V - 0.6V \pm \sqrt{(5V-0.6V)^2 - \left(\frac{0.8mA/V^2}{2.0mA/V^2}\right)(-0.4V)^2} = 0.0073V$$

$$V_{OH} = V_{DD} = 5V.$$

b. The noise margins are

$$V_{NML} = 0.73V - 0.0073V = 0.72V$$

and

$$V_{NMH} = 5V - 0.89V = 4.1V.$$

c. The average dissipation is

$$P_{DC} \approx \frac{P_H + P_L}{2} = \frac{K_L V_{DD} V_{TL}^2}{4} = \frac{(0.8mA/V^2)(5V)(-0.4V)^2}{4} = 0.160mW.$$

P8.2. Consider the NMOS gate of Figure 8.31.

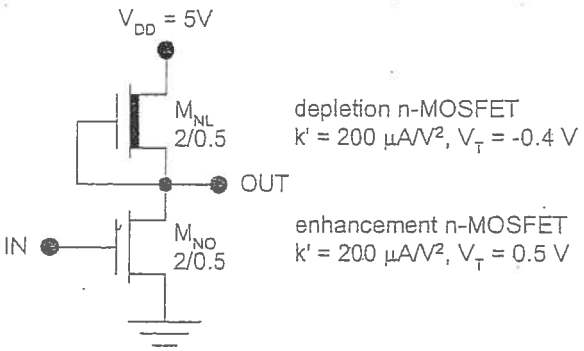

Figure 8.31.

Determine the values of V_{IN} and V_{OUT} for which M_{NO} is at the boundary between saturation and ohmic operation.

Solution. M_{NL} will be saturated so that

$$I_{DD} = \frac{K_L(-V_{TL})^2}{2}.$$

For M_{NO},

$$I_{DD} = \frac{K_O(V_{IN} - V_{TO})^2}{2}.$$

But if M_{NO} is at the boundary between saturated and linear operation, then

$$V_{IN} - V_{TO} = V_{OUT}.$$

Hence

$$\frac{K_L(-V_{TL})^2}{2} = \frac{K_O(V_{OUT})^2}{2} \text{ so that}$$

$$V_{OUT} = 0.4V.$$

P8.3. Consider the NMOS gate illustrated in Figure 8.32.

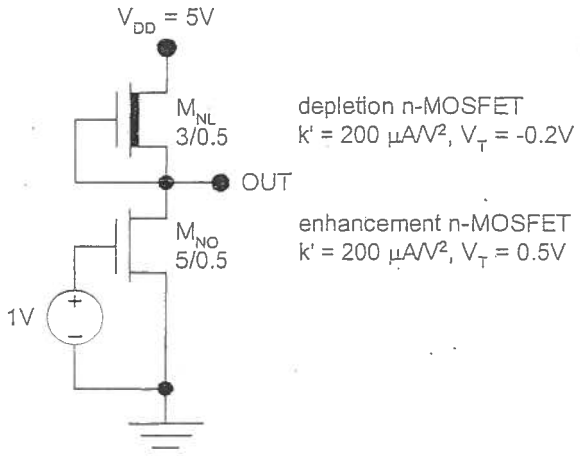

Figure 8.32.

a. Determine the mode of operation for each of the transistors.

b. Determine the supply current I_{DD}.

c. Determine the value of V_{OUT}.

Solution.

a. Assume that M_{NO} is linear and M_{NL} is saturated. Then

$$I_{DD} = \frac{1.2mA/V^2}{2}(0.2V)^2 = 0.024mA$$

and

$$V_{OUT} = (1V - 0.5V) - \sqrt{(1V - 0.5V)^2 - \frac{2(0.024mA)}{2mA/V^2}} = 0.025V .$$

This is consistent with the starting assumptions.

b. The supply current is

$$I_{DD} = 0.024mA .$$

c. The output voltage is

$V_{OUT} = 0.025V$.

P8.4. Consider the NMOS gate of Figure 8.33.

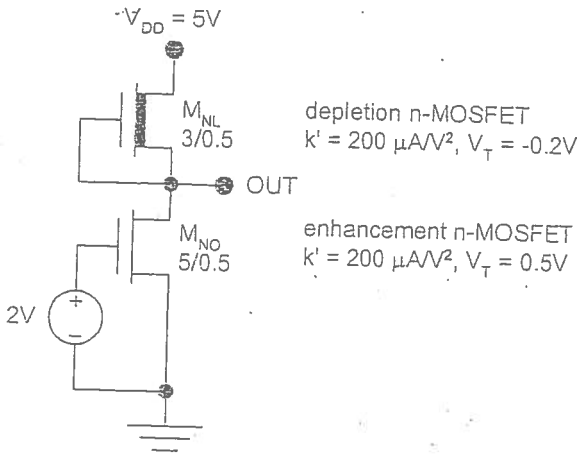

Figure 8.33.

a. Determine the mode of operation for each of the transistors.

b. Determine the supply current I_{DD}.

c. Determine the value of V_{OUT}.

Solution. The device transconductance parameters are given by

$$K_L = \left(\frac{3\mu m}{0.5\mu m}\right)200\mu A/V^2 = 1.2mA/V^2 \text{ and}$$

$$K_O = \left(\frac{5\mu m}{0.5\mu m}\right)200\mu A/V^2 = 2.0mA/V^2.$$

a. Suppose M_{NL} is saturated but M_{NO} is linear. Then

$$I_{DD} = \frac{(1.2mA/V^2)(0.2V)^2}{2} = 0.024mA$$

and

$$V_{OUT} = (2V - 0.5V) - \sqrt{(2V - 0.5V)^2 - \frac{2(0.024mA)}{2.0mA/V^2}} = 0.0080V .$$

Therefore $V_{DSO} < V_{GSO}-V_{TO}$ but $V_{DSL} > V_{GSL}-V_{TL}$, consistent with the starting assumptions.

b. The supply current is

$$I_{DD} = 0.024mA .$$

c. The output voltage is

$$V_{OUT} = 0.0080V .$$

P8.5. Consider the NMOS gate illustrated in Figure 8.34.

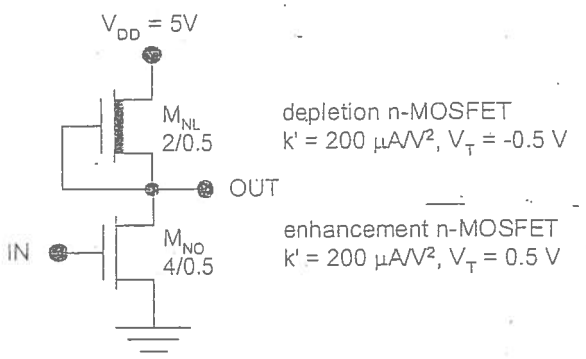

Figure 8.34.

a. Using hand calculations, determine and plot the voltage transfer characteristic for the inverter.

b. Determine the range of V_{IN} for each mode of operation (cutoff, saturation, and linear) of M_{NO}.

Solution. The device transconductance parameters are given by

$$K_L = \left(\frac{2\mu m}{0.5\mu m}\right) 200\mu A/V^2 = 0.8mA/V^2 \text{ and}$$

$$K_O = \left(\frac{4\mu m}{0.5\mu m}\right) 200\mu A/V^2 = 1.6mA/V^2.$$

For $V_{IN} \leq 0.5V$, M_{NO} is cut off and M_{NL} is linear, so that

$$V_{OUT} = 5V \quad (V_{IN} \leq 0.5V).$$

If $(V_{OUT} + 0.5V) \leq V_{IN} \leq 0.5V$ and $V_{OUT} \geq 4.5V$, M_{NO} is saturated and M_{NL} is linear so that

$$I_{DD} = \frac{K_O}{2}(V_{IN} - V_{TO})^2, \text{ and}$$

$$V_{OUT} = V_{DD} - V_{DSL} = V_{DD} - \left[-V_{TL} - \sqrt{(-V_{TL})^2 - \frac{K_O(V_{IN} - V_{TO})^2}{K_L}}\right]$$

$$= 4.5V + \sqrt{(0.5V)^2 - (2)(V_{IN} - 0.5V)^2};$$

$$[(V_{OUT} + 0.5V) \leq V_{IN} \leq 0.5V] \text{ and } [V_{OUT} \geq 4.5V]$$

Finally, if M_{NO} is linear and M_{NL} is saturated then

$$I_{DD} = \frac{K_L}{2}(-V_{TL})^2, \text{ and}$$

$$V_{OUT} = V_{DSO} = (V_{IN} - V_{TO}) - \sqrt{(V_{IN} - V_{TO})^2 - \frac{K_L(-V_{TL})^2}{K_O}} -$$

$$= V_{IN} - 0.5V - \sqrt{(V_{IN} - 0.5V)^2 - (-0.5)^2/2};$$

$$[(V_{OUT} + 0.5V) \geq V_{IN}] \text{ and } [V_{OUT} \leq 4.5V]$$

The voltage transfer characteristic appears in Figure 8.40.

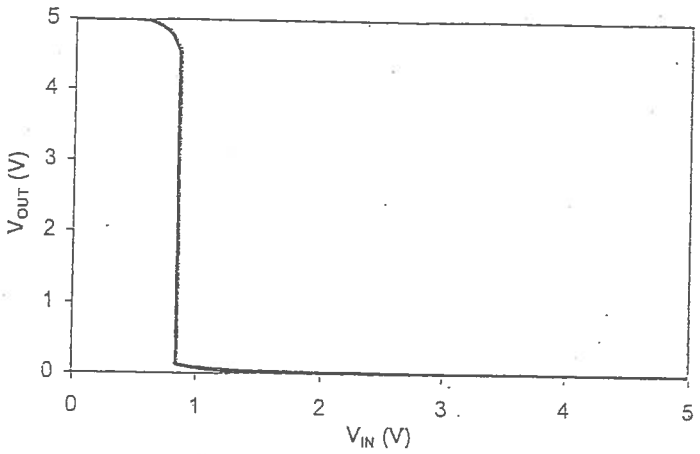

Figure 8.40.

b. The ranges of V_{IN} for each mode of operation (cutoff, saturation, and linear) of M_{NO} are as follows:

M_{NO} is cutoff for $V_{IN} \leq 0.5V$.

M_{NO} is saturated for $0.5 \leq V_{IN} \leq 0.853V$.

M_{NO} is linear for $0.853 \leq V_{IN}$.

P8.6. Consider the NMOS gate shown in Figure 8.35.

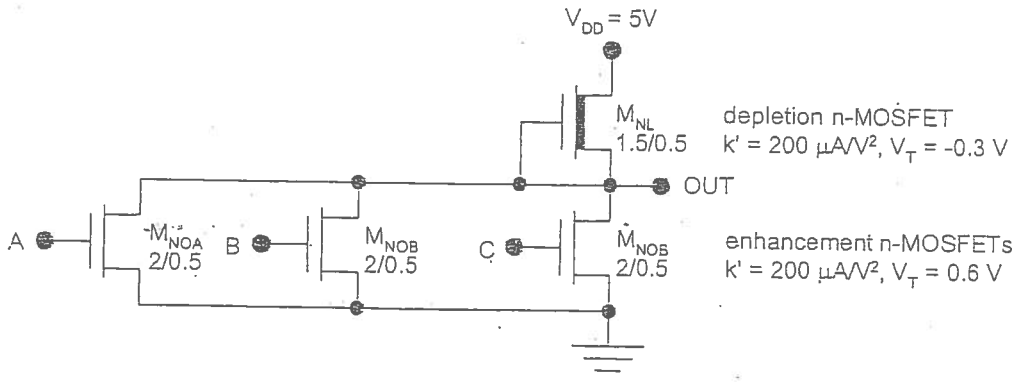

Figure 8.35.

a. Determine the value of V_{OUT} if $V_A = 5V$ and $V_B = V_C = 0V$. (This is the worst case of V_{OL}.)

b. Determine the value of V_{OUT} if $V_A = V_B = V_C = 5V$.

Solution.

a. With $V_{INA} = 5V$ and $V_{INB} = V_{INC} = 0V$,

$$V_{OL}(\text{one transistor on}) = V_{DD} - V_{TO} - \sqrt{(V_{DD} - V_{TO})^2 - \left(\frac{K_L}{K_O}\right)V_{TL}^2}$$

$$= 5V - 0.6V - \sqrt{(5V - 0.6V)^2 - \left(\frac{1.5/0.5}{2/0.5}\right)(-0.3V)^2} = 0.0075V$$

b. With $V_{INA} = V_{INB} = V_{INC} = 5V$,

$$V_{OL}(3 \text{ transistors on}) = V_{DD} - V_{TO} - \sqrt{(V_{DD} - V_{TO})^2 - \left(\frac{K_L}{3K_O}\right)V_{TL}^2}$$

$$= 5V - 0.6V - \sqrt{(5V - 0.6V)^2 - \left(\frac{1.5/0.5}{(3)2/0.5}\right)(-0.3V)^2} = 0.0025V$$

P8.7. Consider the NMOS NAND3 gate illustrated in Figure 8.36.

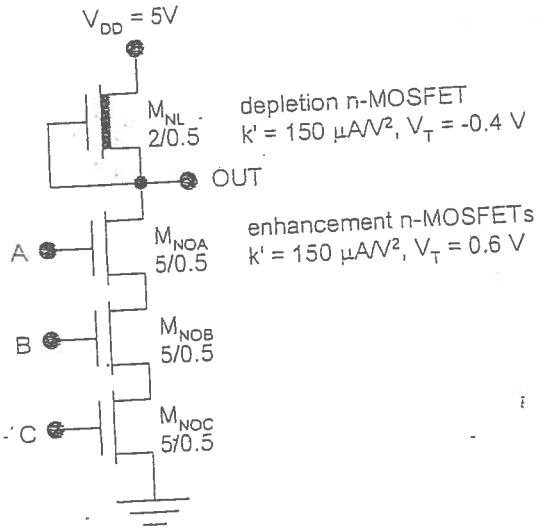

Figure 8.36.

Determine the value of V_{OL}.

Solution. For the NAND3 gate,

$$V_{OL} = V_{DD} - V_{TO} - \sqrt{(V_{DD} - V_{TO})^2 - 3\left(\frac{K_L}{K_O}\right)V_{TL}^2}$$

$$= 5V - 0.6V - \sqrt{(5V - 0.6V)^2 - 3\left(\frac{5}{2}\right)(-0.4V)^2} = 0.138V$$

P8.8. Consider the NMOS gate depicted in Figure 8.37.

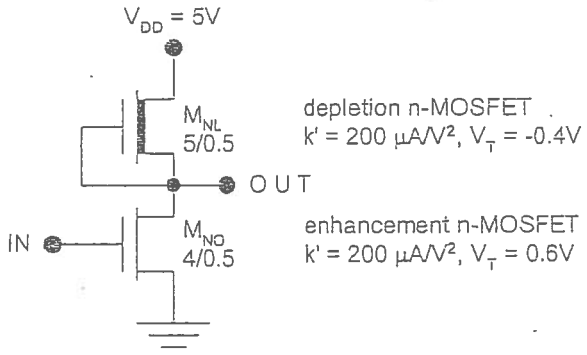

Figure 8.37.

a. Using hand calculations, determine V_{IL}, V_{IH}, V_{OL}, and V_{OH}.

b. Using SPICE, determine and plot the voltage transfer characteristic for the gate.

c. From the tabulated SPICE results, determine the critical voltages and compare these to the values found in (a).

Solution.

a. The device transconductance parameters are given by

$$K_L = \left(\frac{5\mu m}{0.5\mu m}\right)200\mu A/V^2 = 2.0mA/V^2 \text{ and}$$

$$K_O = \left(\frac{4\mu m}{0.5\mu m}\right)200\mu A/V^2 = 1.6mA/V^2.$$

The four critical voltages are

$$V_{IL} = V_{TO} + \frac{K_L}{\sqrt{K_O K_L + K_O^2}}|V_{TL}|$$

$$= 0.6V + \frac{2.0mA/V^2}{\sqrt{(1.6mA/V^2)(2.0mA/V^2) + (1.6mA/V^2)^2}}|-0.4V| = 0.93V$$

$$V_{IH} = V_{TO} + 2|V_{TL}|\sqrt{\frac{K_L}{3K_O}} = 0.6V + 2|-0.4V|\sqrt{\frac{2.0mA/V^2}{3(1.6mA/V^2)}} = 1.12V,$$

$$V_{OL} = V_{DD} - V_{TO} - \sqrt{(V_{DD} - V_{TO})^2 - \left(\frac{K_L}{K_O}\right)V_{TL}^2}$$

, and

$$= 5V - 0.6V - \sqrt{(5V - 0.6V)^2 - \left(\frac{2.0mA/V^2}{1.6mA/V^2}\right)(-0.4V)^2} = 0.023V$$

$$V_{OH} = V_{DD} = 5V.$$

b. The SPICE results are shown in Figure 8.41.

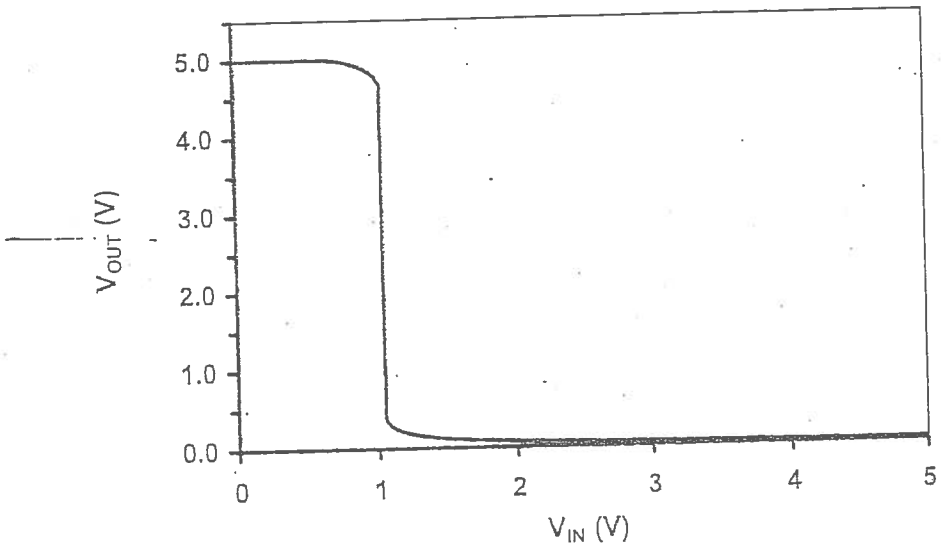

Figure 8.41.

c. From the SPICE results, the critical voltages are $V_{OH} = 5.0V$, $V_{OL} = 0.023V$, $V_{IL} = 0.88V$ and $V_{IH} = 1.12V$.

P8.9. Consider the NMOS gate of Figure 8.38.

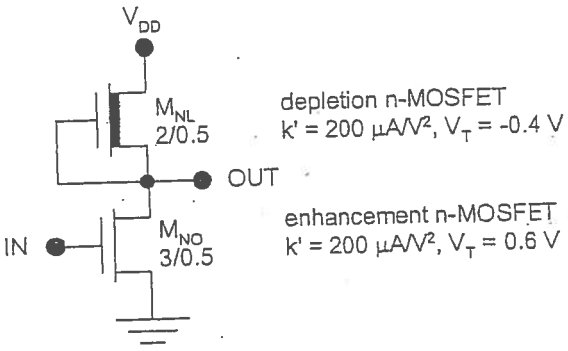

Figure 8.38.

a. Using hand calculations, calculate and plot the DC power dissipation versus the supply voltage.

b. Repeat using SPICE. Plot the results together on one graph for comparison.

Solution.

a. For the pull-up device,

$$K_L = \left(\frac{2\mu m}{0.5\mu m}\right) 200\mu A/V^2 = 0.8mA/V^2.$$

The dissipation is given by

$$P_{DC} \approx \frac{P_H + P_L}{2} = \frac{K_L V_{DD} V_{TL}^2}{4} = \frac{(0.8mA/V^2)(V_{DD})(-0.4V)^2}{4} = 0.032mW/V(V_{DD}).$$

b. The dissipation was determined as a function of the supply voltage in PSPICE using a DC sweep and a current probe. The calculated and PSPICE results coincide as shown in Figure 8.42.

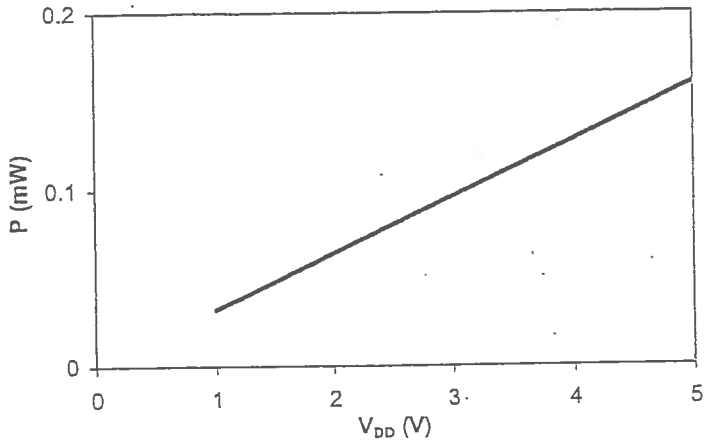

Figure 8.42.

P8.10. Consider the NMOS gate shown in Figure 8.39.

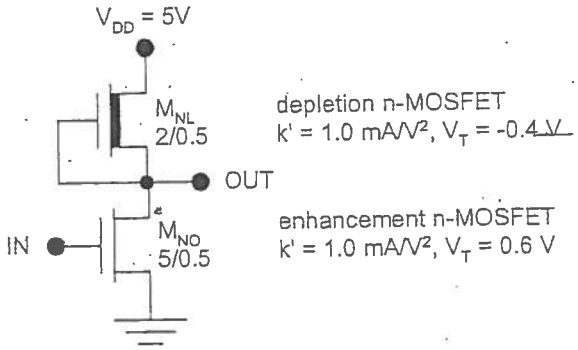

Figure 8.39.

a. From the information given, estimate the oxide thickness used in the transistors.

b. Calculate the approximate input capacitance for the inverter.

c. Estimate the maximum fan-out if $t_{p,max}$ = 10 ns.

Solution.

a. The oxide thickness is

$$t_{ox} = \frac{(580 cm^2 V^{-1} s^{-1})(3.9)(8.85\times10^{-14} F/cm)}{1 mA/V^2} = 2nm$$

b. The input capacitance for the inverter is

$$C_{IN} = \frac{(5\times10^{-4} cm)(0.5\times10^{-4} cm)(3.9)(8.85\times10^{-14} F/cm)}{20\times10^{-8} cm} = 43 fF.$$

c. If $t_{pMAX} = 10$ ns then the maximum fan-out is given by

$$N_{MAX} \le \frac{(4mA/V^2)(0.4V)^2(10^{-8} s)}{(5V)(43 fF)} = 30, \text{ or}$$

$$N_{MAX} = 30.$$

P8.11. Consider depletion loaded NMOS with $V_{DD} = 5V$, $V_{TO} = 0.5V$, $V_{TL} = -0.6V$, and $t_{ox} = 18$ nm. All devices have 0.5 μm gate lengths. Choose the W_O/W_L ratio such that $V_{OL} = 25$ mV.

Solution. The output low voltage is given by

$$V_{OL} = V_{DD} - V_{TO} - \sqrt{(V_{DD} - V_{TO})^2 - \left(\frac{K_L}{K_O}\right)V_{TL}^2}$$

$$= 5V - 0.5V - \sqrt{(5V - 0.5V)^2 - \left(\frac{K_L}{K_O}\right)(-0.6V)^2} = 0.025V$$

Therefore the ratio of the device transconductance parameters should be

$$\frac{K_L}{K_O} = \frac{(V_{DD} - V_{TO})^2 - (V_{DD} - V_{TO} - V_{OL})^2}{V_{TL}^2}$$

$$= \frac{(5V - 0.5V)^2 - (5V - 0.5V - 0.025V)^2}{(-0.6V)^2} = 0.62$$

The ratio of the device widths should be

$$\frac{W_O}{W_L} = \frac{K_O}{K_L} = \frac{1}{0.62} = 1.61.$$

P8.12. Consider depletion loaded NMOS with V_{DD} = 3.3V, V_{TO} = 0.5V, V_{TL} = -0.3V, and t_{ox} = 10 nm. All devices have 0.35 μm gate lengths. Design the transistors for the inverter (choose W_O and W_L) such that V_{OL} = 20 mV and the average DC dissipation is 2 mW.

Solution. The DC power dissipation is given by

$$P_{DC} \approx \frac{P_H + P_L}{2} = \frac{K_L V_{DD} V_{TL}^2}{4} = 2mW .$$

Therefore the value of K_L can be chosen as

$$K_L = \frac{(4)(2mW)}{(3.3V)(-0.3V)^2} = 27mA/V^2 .$$

The output low voltage is given by

$$V_{OL} = V_{DD} - V_{TO} \pm \sqrt{(V_{DD} - V_{TO})^2 - \left(\frac{K_L}{K_O}\right) V_{TL}^2}$$

$$= 3.3V - 0.5V \pm \sqrt{(3.3V - 0.5V)^2 - \left(\frac{K_L}{K_O}\right)(-0.3V)^2} = 0.020V$$

Therefore,

$$\frac{K_L}{K_O} = 1.24 \text{ and}$$

$$K_O = 22mA/V^2 .$$

The process transconductance parameter is

$$k_N' = \frac{(580cm^2/Vs)(3.9)(8.85\times10^{-14} F/cm)}{100\times10^{-8} cm} = 0.200mA/V^2 .$$

The widths for the devices should therefore be:

$$W_L = \left(\frac{27mA/V^2}{0.20mA/V^2}\right)0.35\mu m = 47\mu m \text{, and}$$

$$W_O = \left(\frac{22mA/V^2}{0.20mA/V^2}\right)0.35\mu m = 38\mu m .$$

P8.13. Consider depletion loaded NMOS with V_{DD} = 3.3V, V_{TO} = 0.5V, V_{TL} = -0.3V, and t_{ox} = 10 nm. All devices have 0.35 μm gate lengths. Design the transistors for the inverter (choose W_O and W_L) such that V_{OL} = 20 mV and $t_P \leq 10$ ns with C_L = 15 pF. (Consider the worst case propagation delay.)

Solution.

$$V_{OL} = V_{DD} - V_{TO} \pm \sqrt{(V_{DD} - V_{TO})^2 - \left(\frac{K_L}{K_O}\right)V_{TL}^2}$$

$$= 3.3V - 0.5V \pm \sqrt{(3.3V - 0.5V)^2 - \left(\frac{K_L}{K_O}\right)(-0.3V)^2} = 0.020V$$

$$\frac{K_L}{K_O} = 1.24$$

$$t_{PLH} = \frac{V_{DD}C_L}{K_L V_{TL}^2} = \frac{(3.3V)(15pF)}{1.24K_O(-0.3V)^2} = \frac{0.44nsA/V^2}{K_O}.$$

The high to low propagation delay is

$$t_{PHL} \approx \frac{V_{DD}C_L}{K_O(V_{DD} - V_{TO})^2} = \frac{(3.3V)(15pF)}{K_O(3.3V - 0.5V)^2} = \frac{0.0063nsA/V^2}{K_O}.$$

Considering the worst case, which is t_{PLH},

$$K_O \geq \frac{0.44nsA/V^2}{10ns} = 0.044A/V^2$$