Problem Solutions

Chapter Five: Transistor-Transistor Logic

P5.1. For the *unloaded* RTL inverter of Figure 5.82, determine the value of the input voltage for which $V_{OUT} = V_{IN}$.

Solution. This occurs with the output voltage greater than V_{BEA}, so the transistor will be forward active. Therefore

$$V_{OUT} = V_{CC} - \left(\frac{V_{IN} - V_{BEA}}{R_B}\right)\beta_F R_C .$$

But

$V_{OUT} = V_{IN}$, so that

$$V_{IN} = V_{CC} - \left(\frac{V_{IN} - V_{BEA}}{R_B}\right)\beta_F R_C .$$

Solving,

$$V_{IN} = \frac{V_{CC} + V_{BEA}\beta_F R_C / R_B}{1 + \beta_F R_C / R_B} = \frac{5.5V + 0.7V(70)(3k\Omega)/7.5k\Omega}{1 + (70)(3k\Omega)/7.5k\Omega} = 0.87V .$$

P5.2. For the *unloaded* RTL inverter of Figure 5.83, $V_{IN} = 1.1V$ as shown. No load gates are connected.

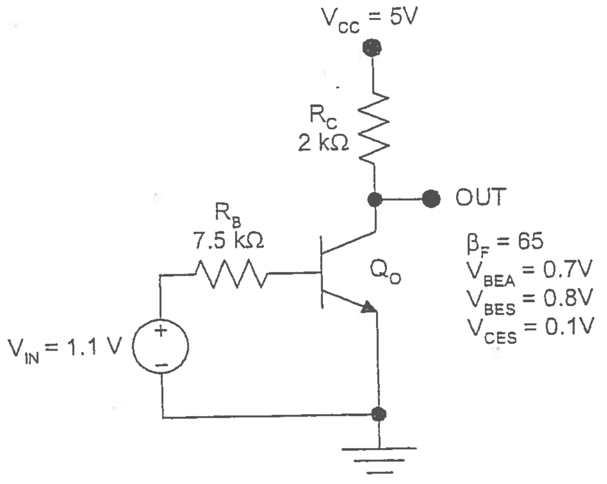

Figure 5.83.

a. Determine the mode of operation for the transistor.

b. Determine the supply current I_{CC}.

c. Determine the output voltage V_{OUT}.

Solution. If it is assumed that the transistor is forward active, then

$$I_B = \frac{1.1V - 0.7V}{7.5k\Omega} = 0.053mA,$$

$I_C = (65)(0.053mA) = 3.4mA$, and

$V_{OUT} = 5V - (3.4mA)(2k\Omega) = -1.8V$.

This is not possible so the starting assumption was incorrect and the transistor will be saturated.

a. saturation

b. $I_{CC} = \dfrac{5V - 0.1V}{2k\Omega} = 2.4mA$, and

c. $V_{OUT} = 0.1V$.

P5.3. For the RTL NOR gate of Figure 5.84, the inputs are as shown. Assume N = 5.

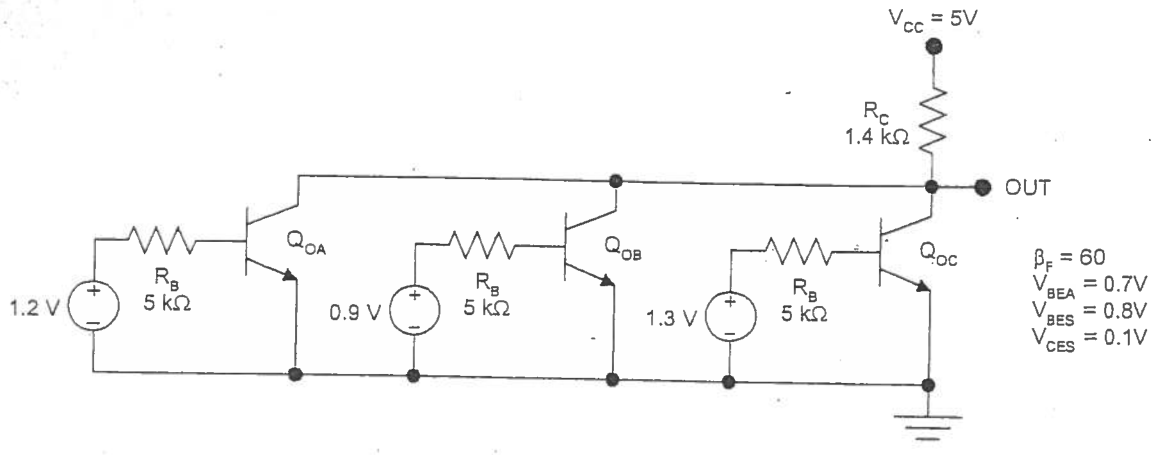

Figure 5.84.

a. Determine the mode of operation for each of the three transistors.

b. Determine the supply current I_{CC}.

c. Determine the output voltage V_{OUT}.

Solution. If it is assumed that all three transistors are forward active, then

$$I_{CC} = I_{C1} + I_{C2} + I_{C3}$$

$$= 60\left(\frac{1.2V - 0.7V}{5k\Omega} + \frac{0.9V - 0.7V}{5k\Omega} + \frac{1.3V - 0.7V}{5k\Omega}\right) = 15.6mA$$

However, the maximum current which can flow in R_C is

$$I_{CC,\max} = \frac{5V - 0.1V}{1.4k\Omega} = 3.5mA.$$

Therefore, the transistors will all saturate.

a. All of the transistors will saturate.

b. $I_{CC} = \dfrac{5V - 0.1V}{1.4k\Omega} = 3.5mA$, and

c. $V_{OUT} = 0.1V$.

P5.4. For the RTL NOR gate of Figure 5.85, determine the maximum fan-out assuming that the minimum value of the high noise margin in 0.1V.

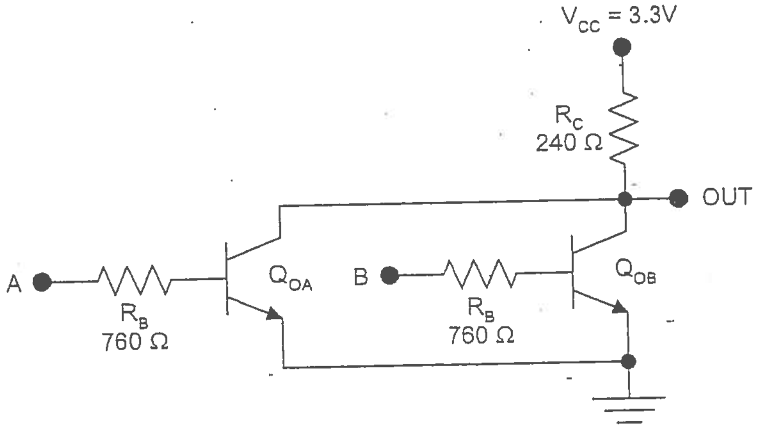

Figure 5.85.

Solution. The maximum fan-out is the largest integer satisfying

$$N_{MAX} \le \frac{V_{CC} - V_{BES} - V_{NMH}(\min) - \dfrac{R_B\left(V_{CC} - V_{CES}\right)}{\beta_F R_C}}{\dfrac{R_C V_{NMH}(\min)}{R_B} + \dfrac{V_{CC} - V_{CES}}{\beta_F}}, \text{ or}$$

$$N_{MAX} \le \frac{3.3V - 0.8V - 0.1V - \dfrac{0.76k\Omega(3.3V - 0.1V)}{(70)(0.24k\Omega)}}{\dfrac{(0.24k\Omega)(0.1V)}{0.76k\Omega} + \dfrac{3.3V - 0.1V}{70}} = 29.2.$$

Therefore

$$N_{MAX} = 29.$$

P5.5. Consider the RTL gate shown in Figure 5.86.

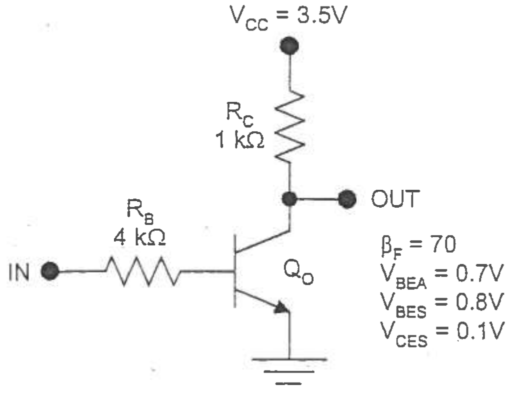

Figure 5.86.

a. Use SPICE to calculate and plot the unloaded VTC for this gate.

b. Hand calculate the unloaded VTC, and plot it on the same graph as the SPICE results. Compare the SPICE and hand calculations.

Solution. The inverter was assumed to be unloaded.

a. For the SPICE simulation, the emission coefficients were assumed to be unity and the saturation current was estimated assuming that the base-emitter voltage of 0.7V corresponds to an emitter current of 1 mA. Hence

$$I_S = \frac{10^{-3}A}{\exp(0.7V/0.026V)} = 2.0\times10^{-15}A.$$

b. The critical voltages were hand-calculated as follows:

$$V_{IL} = V_{BEA} = 0.7V,$$

$$V_{IH} = V_{BES} + \frac{R_B(V_{CC} - V_{CES})}{\beta_F R_C} = 0.8V + \frac{4k\Omega(3.5V - 0.1V)}{(70)(1k\Omega)} = 0.99V,$$

$$V_{OL} = V_{CES} = 0.1V, \text{ and}$$

$$V_{OH} = V_{CC} = 3.5V.$$

The SPICE and hand-calculated voltage transfer characteristics appear in Figure 5.117.

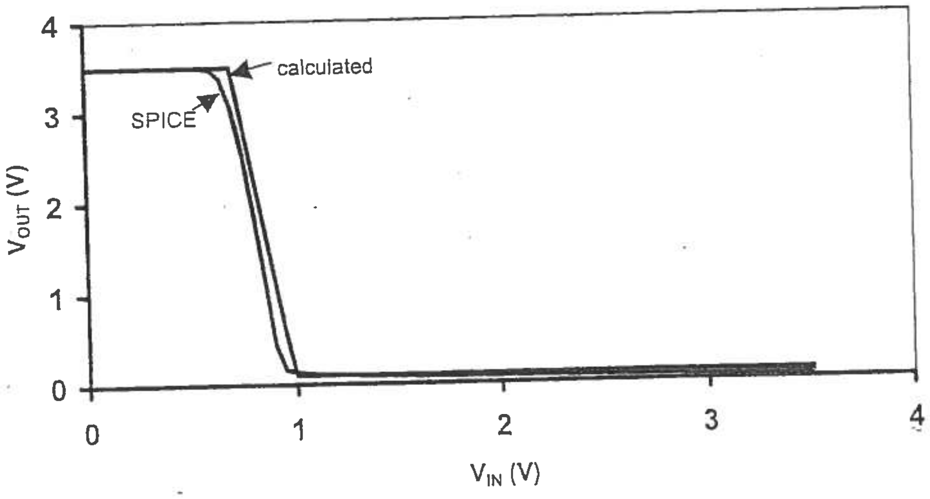

Figure 5.117.

P5.6. Consider the *unloaded* RTL gate of Figure 5.87.

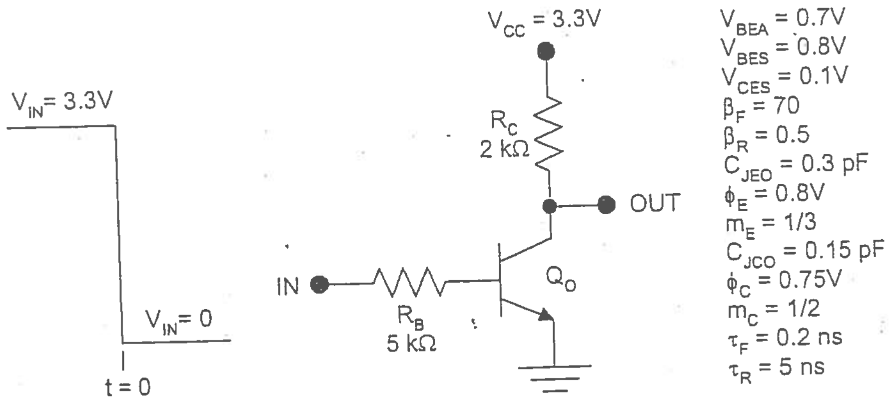

Figure 5.87.

a. Estimate the saturation delay.

b. Estimate the rise time.

c. Estimate the low-to-high propagation delay.

Solution.

a. The saturation time constant is

$$\tau_S = \frac{\alpha_F(\tau_F + \alpha_R\tau_R)}{1-\alpha_F\alpha_R} = \frac{0.986(0.2ns + (0.333)5ns)}{1-(0.986)(0.333)} = 2.7ns\ .$$

The saturated base current is

$$I_{BF} = \frac{V_{CC} - V_{BES}}{R_B} = \frac{3.3V - 0.8V}{5k\Omega} = 0.5mA\,.$$

During the saturation delay, the base current is

$$I_{BR} = \frac{0 - V_{BES}}{R_B} = \frac{0-0.8V}{5k\Omega} = -0.16mA\,.$$

The collector current at the edge of saturation is

$$I_{CEOS} = \frac{V_{CC} - V_{CES}}{R_C} = \frac{3.3V - 0.1V}{2k\Omega} = 1.6mA\,.$$

The saturation delay is therefore

$$t_S = \tau_S \ln\left(\frac{I_{BF} - I_{BR}}{I_{CEOS}/\beta_F - I_{BR}}\right) = 2.7ns\ln\left(\frac{0.5mA-(-0.16mA)}{1.6mA/70-(-0.16mA)}\right) = 3.5ns$$

b. For the calculation of the rise time, the base-collector voltage starts at +0.7V and ends up at –2.6V. Therefore the average value of the base-collector capacitance for the rise time calculation is

$$C_{BC} = \frac{C_{JCO}\phi_C}{(V_{BC1} - V_{BC2})(1-m_C)}\left[\left(1-\frac{V_{BC2}}{\phi_C}\right)^{1-m_C} - \left(1-\frac{V_{BC1}}{\phi_C}\right)^{1-m_C}\right]$$

$$= \frac{(0.15pF)(0.75V)}{(0.7V-(-2.6V))(0.5)}\left[\left(1-\frac{-2.6V}{0.75V}\right)^{0.5} - \left(1-\frac{0.7V}{0.75V}\right)^{0.5}\right] = 0.104pF$$

The base current during the rise time is

$$I_B(ave) = \frac{0 - V_{BEA}}{R_B} = \frac{0-0.7V}{5k\Omega} = -0.14mA\,.$$

The rise time is

$$t_R = \frac{I_{CEOS}\tau_F + |\Delta V_{BC} C_{BC}|}{|I_B(ave)|} = \frac{(1.6mA)0.2ns + |(-2.6V - 0.7V)(0.104pF)|}{|-0.14mA|} = 4.7ns.$$

c. The low-to-high propagation delay is

$$t_{PLH} = t_S + \frac{t_R}{2} = 3.5ns + \frac{4.7ns}{2} = 5.8ns.$$

P5.7. Consider the *unloaded* RTL gate depicted in Figure 5.88.

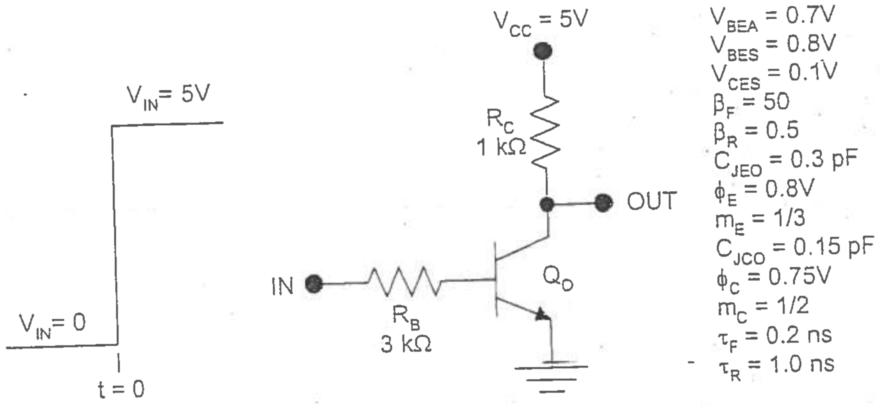

Figure 5.88.

a. Estimate the delay time.

b. Estimate the fall time.

c. Estimate the high-to-low propagation delay.

Solution.

a. To determine the delay time, we must first calculate the average base current, and the average values of C_{BE} and C_{BC}. The base voltage rises from zero to 0.7V so the average base current is

$$I_B(ave) = \frac{V_{CC} - V_{BEA}/2}{R_B} = \frac{3.3V - 0.7V/2}{5k\Omega} = 0.59mA.$$

The base-emitter voltage increases from zero to 0.7V so the average value of the base-emitter capacitance is

$$C_{BE} = \frac{C_{JEO}\phi_E}{(V_{BE1} - V_{BE2})(1-m_E)}\left[\left(1-\frac{V_{BE2}}{\phi_E}\right)^{1-m_E} - \left(1-\frac{V_{BE1}}{\phi_E}\right)^{1-m_E}\right]$$

$$= \frac{(0.3pF)(0.8V)}{(0-0.7V)(0.667)}\left[\left(1-\frac{0.7V}{0.8V}\right)^{0.667} - 1\right] = 0.386pF$$

The base-collector voltage starts at –5V and ends up at –4.3V at the end of the delay time. Therefore the average value of the base-collector capacitance for the delay time calculation is

$$C_{BC} = \frac{C_{JCO}\phi_C}{(V_{BC1} - V_{BC2})(1-m_C)}\left[\left(1-\frac{V_{BC2}}{\phi_C}\right)^{1-m_C} - \left(1-\frac{V_{BC1}}{\phi_C}\right)^{1-m_C}\right]$$

$$= \frac{(0.15pF)(0.75V)}{(-5V-(-4.3V))(0.5)}\left[\left(1-\frac{-4.3V}{0.75V}\right)^{0.5} - \left(1-\frac{-5V}{0.75V}\right)^{0.5}\right] = 0.0559pF$$

The delay time is therefore

$$t_D = \frac{V_{BEA}(C_{BE} + C_{BC})}{I_B(ave)} = \frac{0.7V(0.386pF + 0.0559pF)}{0.59mA} = 0.52ns\ .$$

b. For the calculation of the fall time, the base-collector voltage starts at –4.3V and ends up at +0.7V. Therefore the average value of the base-collector capacitance for the fall time calculation is

$$C_{BC} = \frac{C_{JCO}\phi_C}{(V_{BC1} - V_{BC2})(1-m_C)}\left[\left(1-\frac{V_{BC2}}{\phi_C}\right)^{1-m_C} - \left(1-\frac{V_{BC1}}{\phi_C}\right)^{1-m_C}\right]$$

$$= \frac{(0.15pF)(0.75V)}{(-4.3V-(0.7V))(0.5)}\left[\left(1-\frac{0.7V}{0.75V}\right)^{0.5} - \left(1-\frac{-4.3V}{0.75V}\right)^{0.5}\right] = 0.105pF$$

Also

$$I_{CEOS} = \frac{V_{CC} - V_{CES}}{R_C} = \frac{5V - 0.1V}{1k\Omega} = 4.9mA,$$

and for the fall time calculation,

$$I_B(ave) = \frac{V_{CC} - V_{BEA}}{R_B} = \frac{5V - 0.7V}{3k\Omega} = 1.43mA .$$

Therefore the fall time is

$$t_F = \frac{I_{CEOS}\tau_F + \Delta V_{BC}C_{BC}}{I_B(ave)}$$
$$= \frac{(4.9mA)(0.2ns) + (0.7V - (-4.3V))(0.104pF)}{1.43mA} = 1.00ns$$

c. The unloaded high-to-low propagation delay is therefore

$$t_{PHL} = t_D + \frac{t_F}{2} = 0.52ns + \frac{1.00ns}{2} = 1.02ns .$$

P5.8. Consider the RTL inverter of Figure 5.89 with a *lumped capacitive load.*

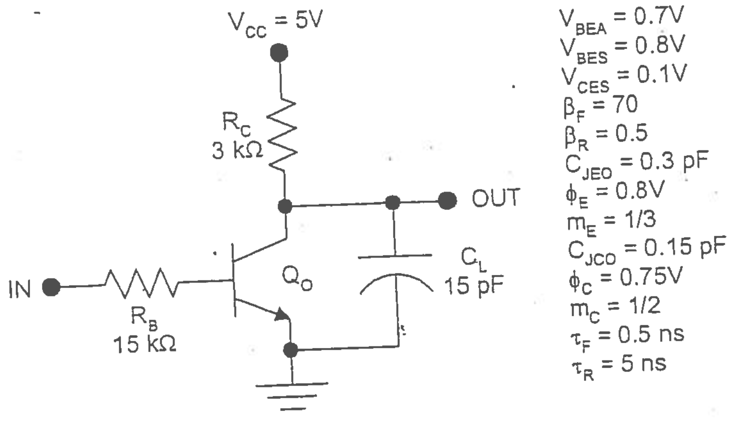

Figure 5.89.

a. Estimate the saturation delay.

b. Estimate the low-to-high propagation delay.

Solution.

a. The saturation time constant is

$$\tau_S = \frac{\alpha_F(\tau_F + \alpha_R\tau_R)}{1-\alpha_F\alpha_R} = \frac{0.986(0.5ns + (0.333)5ns)}{1-(0.986)(0.333)} = 3.2ns\ .$$

The saturated base current is

$$I_{BF} = \frac{V_{CC} - V_{BES}}{R_B} = \frac{5V - 0.8V}{15k\Omega} = 0.28mA\,.$$

During the saturation delay, the base current is

$$I_{BR} = \frac{0 - V_{BES}}{R_B} = \frac{0 - 0.8V}{15k\Omega} = -0.053mA\,.$$

The collector current at the edge of saturation is

$$I_{CEOS} = \frac{V_{CC} - V_{CES}}{R_C} = \frac{5V - 0.1V}{3k\Omega} = 1.63mA\,.$$

The saturation delay is therefore

$$t_S = \tau_S \ln\left(\frac{I_{BF} - I_{BR}}{I_{CEOS}/\beta_F - I_{BR}}\right) = 3.2ns \ln\left(\frac{0.28mA - (-0.053mA)}{1.63mA/70 - (-0.053mA)}\right) = 4.7ns$$

b. The low-to-high propagation delay is

$$t_{PLH} = t_S + R_C C_L \ln 2 = 4.7ns + (3k\Omega)(15pF)\ln 2 = 35.9ns\,.$$

P5.9. For the RTL inverter of Figure 5.90 with a *lumped capacitive load*, determine and plot the low-to-high propagation delay as a function of C_L.

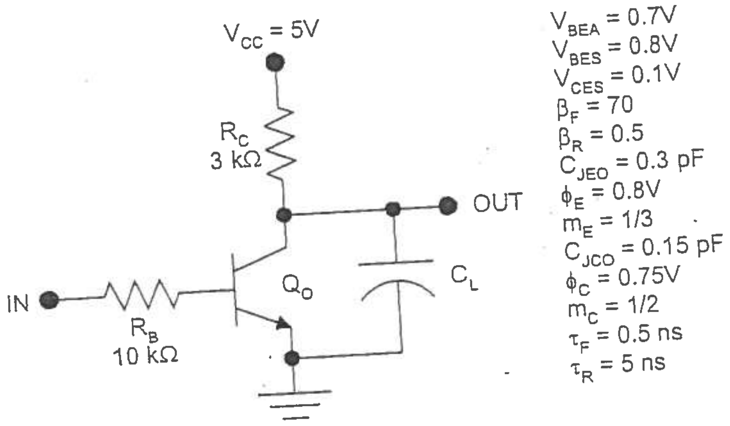

Figure 5.90.

Solution. The saturation time constant is

$$\tau_S = \frac{\alpha_F(\tau_F + \alpha_R \tau_R)}{1 - \alpha_F \alpha_R} = \frac{0.986(0.5ns + (0.333)5ns)}{1 - (0.986)(0.333)} = 3.2ns$$

The saturated base current is

$$I_{BF} = \frac{V_{CC} - V_{BES}}{R_B} = \frac{5V - 0.8V}{10k\Omega} = 0.42mA.$$

During the saturation delay, the base current is

$$I_{BR} = \frac{0 - V_{BES}}{R_B} = \frac{0 - 0.8V}{10k\Omega} = -0.08mA.$$

The collector current at the edge of saturation is

$$I_{CEOS} = \frac{V_{CC} - V_{CES}}{R_C} = \frac{5V - 0.1V}{3k\Omega} = 1.63mA.$$

The saturation delay is therefore

$$t_S = \tau_S \ln\left(\frac{I_{BF} - I_{BR}}{I_{CEOS} / \beta_F - I_{BR}}\right) = 3.2ns \ln\left(\frac{0.42mA - (-0.08mA)}{1.63mA / 70 - (-0.08mA)}\right) = 5.0ns$$

The low-to-high propagation delay is

$$t_{PLH} = t_S + R_C C_L \ln 2 = 5.0ns + C_L(2.1ns/pF).$$

The results are plotted in Figure 5.118.

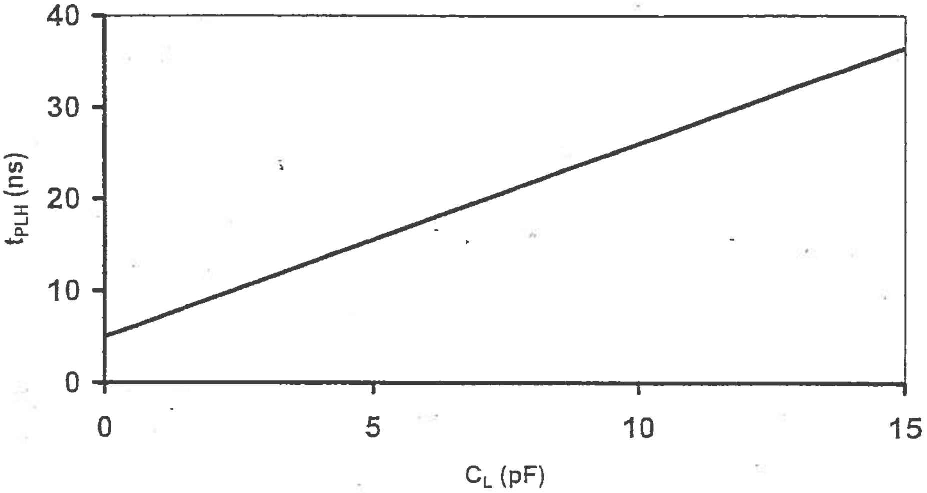

Figure 5.118.

P5.10. Consider a three-stage ring oscillator as shown in Figure 5.91, constructed using DTL inverters as shown in Figure 5.92.

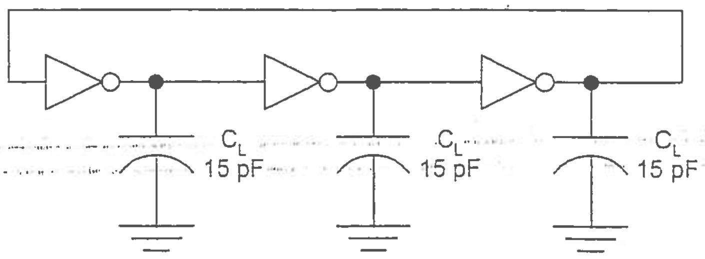

Figure 5.91.

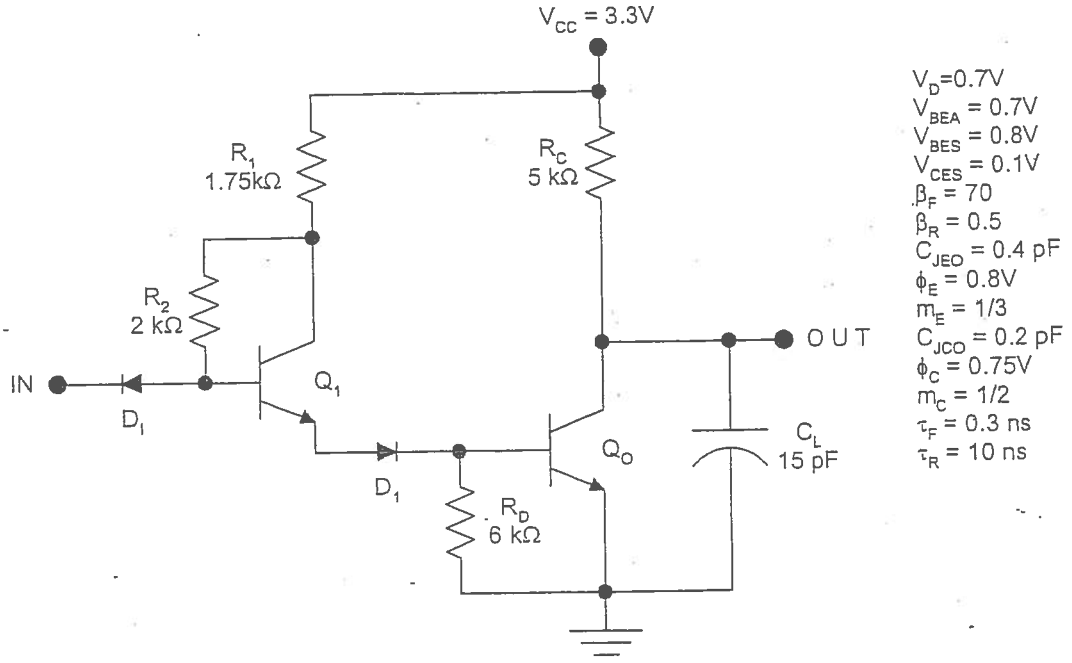

Figure 5.92.

a. Using hand calculations, estimate the oscillation frequency for a three stage ring oscillator constructed using these gates. Assume that each stage is loaded by 15 pF.

b. Using SPICE, determine the oscillation frequency for the same three stage ring oscillator.

Solution.

a. The saturation time constant is

$$\tau_S = \frac{\alpha_F(\tau_F + \alpha_R\tau_R)}{1-\alpha_F\alpha_R} = \frac{0.986(0.3ns + (0.333)10ns)}{1-(0.986)(0.333)} = 5.3ns\ .$$

The saturated base current is

$$I_{BF} = \frac{V_{CC} - V_{BEA} - V_D - V_{BES}}{R_1 + R_2/\beta_F} - \frac{V_{BES}}{R_D}$$

$$= \frac{3.3V - 0.7V - 0.7V - 0.8V}{1.75k\Omega + 2k\Omega/70} - \frac{0.8V}{6k\Omega} = 0.48mA$$

During the saturation delay, the base current is

$$I_{BR} = \frac{0 - V_{BES}}{R_D} = \frac{0 - 0.8V}{6k\Omega} = -0.133mA.$$

The collector current at the edge of saturation is

$$I_{CEOS} = \frac{V_{CC} - V_{CES}}{R_C} = \frac{3.3V - 0.1V}{5k\Omega} = 0.64mA.$$

The saturation delay is therefore

$$t_S = \tau_S \ln\left(\frac{I_{BF} - I_{BR}}{I_{CEOS} / \beta_F - I_{BR}}\right) = 5.3ns \ln\left(\frac{0.48mA - (-0.133mA)}{0.64mA/70 - (-0.133mA)}\right) = 7.7ns$$

The low-to-high propagation delay is

$$t_{PLH} = t_S + R_C C_L \ln 2 = 7.7ns + (5k\Omega)(15pF)\ln 2 = 60ns.$$

Assuming $t_{PLH} >> t_{PHL}$, the three-stage ring oscillator should oscillate at a frequency

$$f = \frac{1}{3(t_{PLH} + t_{PHL})} \approx \frac{1}{3t_{PLH}} = \frac{1}{3(60ns)} = 5.6MHz.$$

b. The results of the SPICE transient simulation are shown in Figure 5.119; the frequency of oscillation is 9.6MHz, or 70% higher than the calculated value.

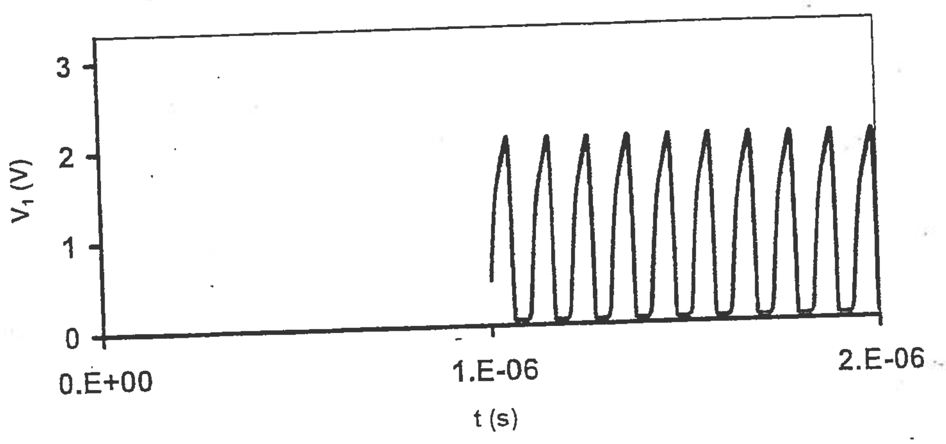

Figure 5.119.

P5.11. Consider the DTL gate of Figure 5.93 with a *lumped capacitive load.*

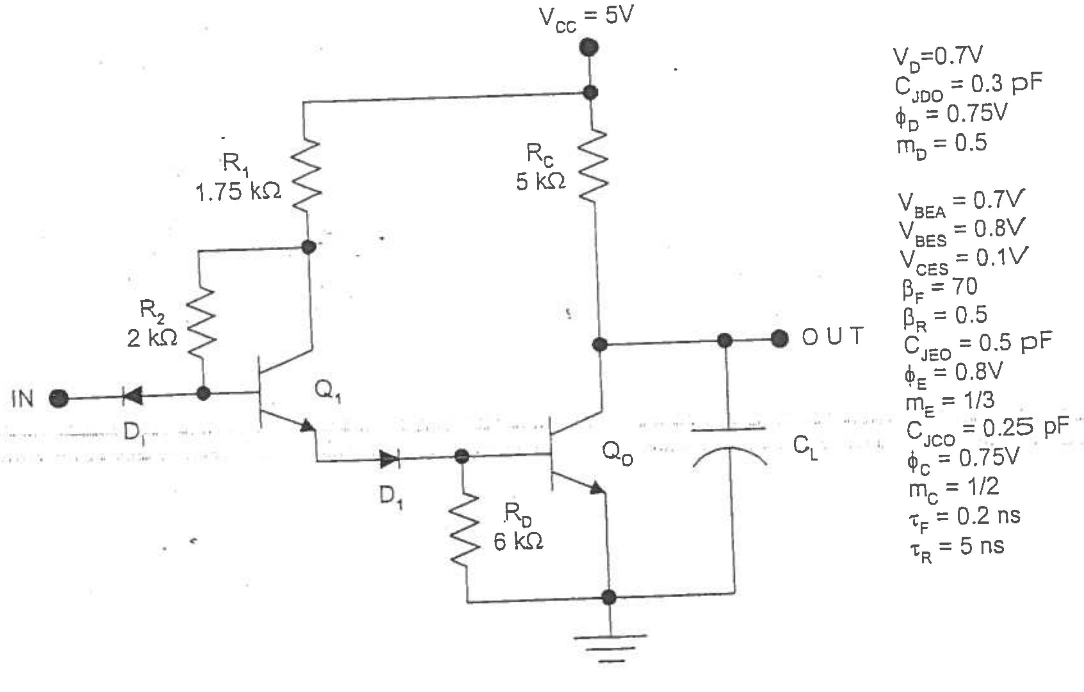

Figure 5.93.

a. Using SPICE, determine and plot t_{PLH} versus C_L.

b. Using SPICE, determine and plot t_{PHL} versus C_L.

c. Determine and plot the average propagation delay versus C_L.

Solution. The results are shown in Figure 5.120.

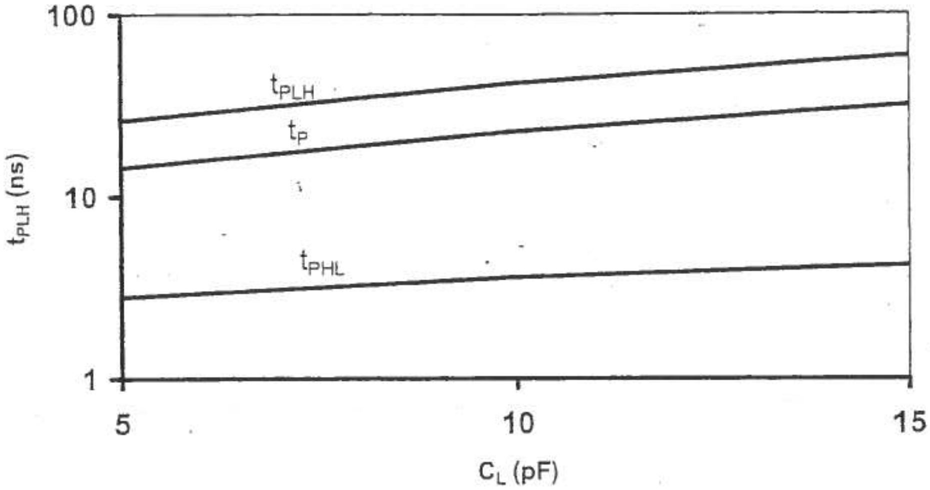

Figure 5.120.

P5.12. Consider the TTL inverter illustrated in Figure 5.94.

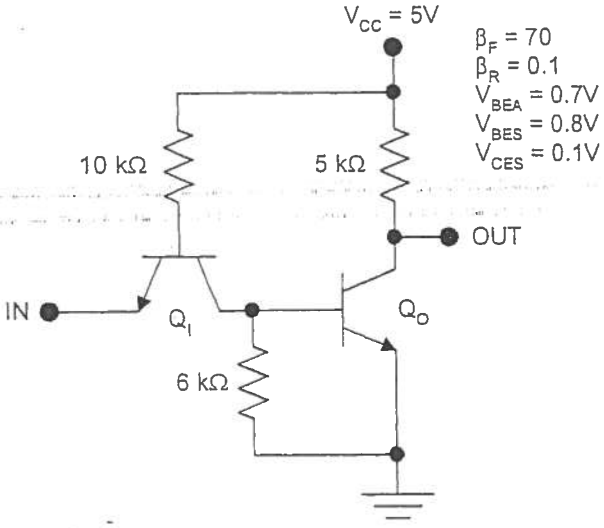

Figure 5.94.

a. Determine V_{IL}, V_{IH}, V_{OL}, and V_{OH}.

b. Determine P_L, P_H, and the average DC dissipation.

c. Determine I_{IL} and I_{IH}.

Solution.

a. The critical voltages are

$V_{IL} = V_{BEA} - V_{CES} = 0.7V - 0.1V = 0.6V$, Q_I sat, Q_o active

$V_{IH} = V_{BES} - V_{CES} = 0.8V - 0.1V = 0.7V$, Q_I sat, Q_O sat.

$V_{OL} = V_{CES} = 0.1V$, and

$V_{OH} = V_{CC} = 5V$.

b. The dissipation is given by

$$P_L = V_{CC}\left(\frac{V_{CC} - V_{BCA} - V_{BES}}{R_B} + \frac{V_{CC} - V_{CES}}{R_C}\right),$$

$$= 5V\left(\frac{5V - 0.7V - 0.8V}{10k\Omega} + \frac{5V - 0.1V}{5k\Omega}\right) = 6.6mW$$

$$P_H = V_{CC}\left(\frac{V_{CC} - V_{BES}}{R_B}\right) = 5V\left(\frac{5V - 0.8V}{10k\Omega}\right) = 2.1mW, \text{ and}$$

$$P_{DC} = \frac{P_L + P_H}{2} = \frac{6.6mW + 2.4mW}{2} = 8.4mW.$$

c. The input low current is

$$I_{IL} = \frac{V_{CC} - V_{BES}}{R_B} = \frac{5V - 0.8V}{10k\Omega} = 0.42mA.$$

The input high current is

$$I_{IH} = \beta_R\left(\frac{V_{CC} - V_{BCA} - V_{BES}}{R_B}\right) = 0.1\left(\frac{5V - 0.7V - 0.8V}{10k\Omega}\right) = 0.035mA.$$

P5.13: Consider the TTL inverter with a steady voltage applied at the input as shown in Figure 5.95.

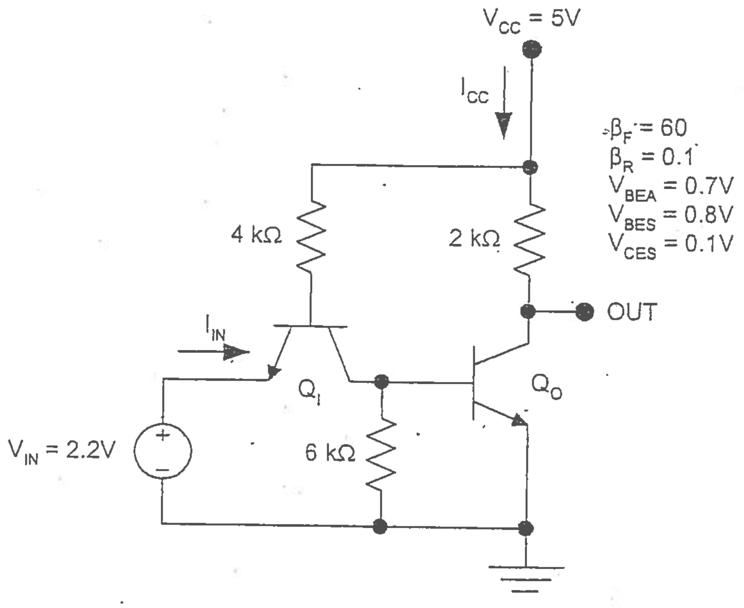

Figure 5.95.

a. Determine the mode of operation for each of the transistors.

b. Determine the supply current I_{CC}.

c. Determine the input current I_{IN}.

d. Determine the output voltage.

Solution.

a. Q_I will be reverse active and Q_O will be saturated.

b. $$I_{CC} = \frac{V_{CC} - V_{BCA} - V_{BES}}{R_B} + \frac{V_{CC} - V_{CES}}{R_C} = \frac{5V - 0.7V - 0.8V}{4k\Omega} + \frac{5V - 0.1V}{2k\Omega} = 3.3mA.$$

c. $$I_{IIN} = \beta_R\left(\frac{V_{CC} - V_{BCA} - V_{BES}}{R_B}\right) = 0.1\left(\frac{5V - 0.7V - 0.8V}{4k\Omega}\right) = 0.088mA.$$

d. $V_{OUT} = V_{CES} = 0.1V$.

P5.14. Consider the standard TTL inverter of Figure 5.96.

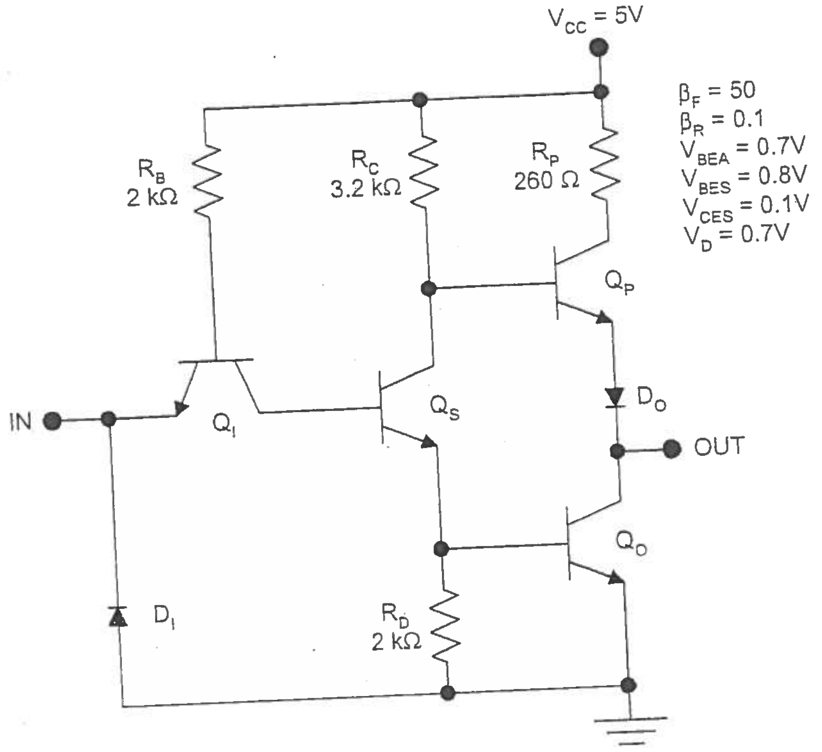

Figure 5.96.

a. Determine and plot the voltage transfer characteristic, showing all critical voltages.

b. Determine P_L, P_H, and the average DC dissipation.

c. Determine I_{IL} and I_{IH}.

d. Determine the maximum fan-out based on DC considerations, assuming $\sigma_{MAX} = ½$.

Solution.

a. At the first breakpoint in the characteristic,

$$V_{IL} = V_{BEA} - V_{CES} = 0.7V - 0.1V = 0.6V\text{, and}$$

$$V_{OH} = V_{CC} - V_{BEA} - V_D = 5V - 0.7V - 0.7V = 3.6V\ .$$

At the second breakpoint,

$V_{IN2} = 2V_{BEA} - V_{CES} = 1.4V - 0.1V = 1.3V$, and

$$V_{OUT2} = V_{CC} - R_C\left(\frac{V_{BEA}}{R_D}\right) - V_{BEA} - V_D = 5V - 3.2k\Omega\left(\frac{0.7V}{2k\Omega}\right) - 0.7V - 0.7V = 2.5V.$$

At the third breakpoint in the voltage transfer characteristic,

$V_{IH} = 2V_{BES} - V_{CES} = 1.6V - 0.1V = 1.5V$, and

$V_{OL} = V_{CES} = 0.1V$.

The entire voltage transfer characteristic is shown in Figure 5.121.

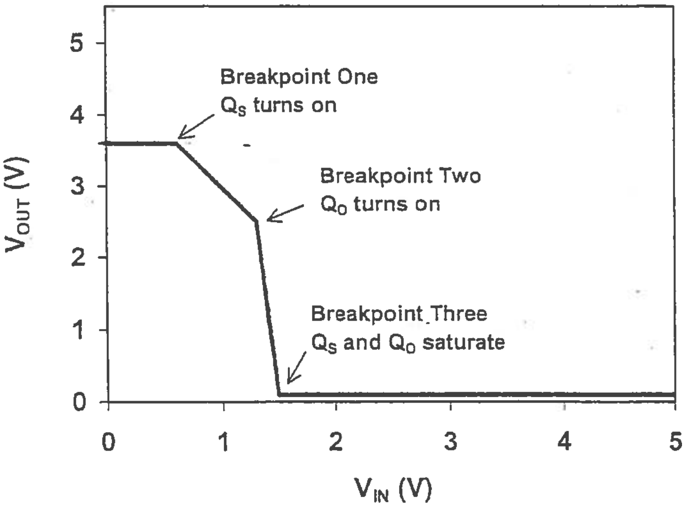

Figure 5.121.

b. The output low power is

$$P_L = V_{CC}\left(\frac{V_{CC} - V_{BCA} - 2V_{BES}}{R_B} + \frac{V_{CC} - V_{CES} - V_{BES}}{R_C}\right)$$

$$= 5V\left(\frac{5V - 0.7V - 1.6V}{2k\Omega} + \frac{5V - 0.1V - 0.8V}{3.2k\Omega}\right) = 13.2mW$$

Assuming the fan-out is zero, the output high power is

$$P_H = V_{CC}\left(\frac{V_{CC} - V_{BES} - V_{CES}}{R_B}\right) = 5V\left[\frac{5V - 0.8V - 0.1V}{2k\Omega}\right] = 10.2mW .$$

Assuming a 50% duty cycle at the output, the average DC power is

$$P_{DC} = \frac{P_L + P_H}{2} = \frac{13.2mW + 10.2mW}{2} = 11.7mW .$$

c. The input low current is

$$I_{IL} = \frac{V_{CC} - V_{BES} - V_{CES}}{R_B} = \frac{5V - 0.8V - 0.1V}{2k\Omega} = 2.05mA .$$

The input high current is

$$I_{IH} = \beta_R\left(\frac{V_{CC} - V_{BCA} - 2V_{BES}}{R_B}\right) = 0.1\left(\frac{5V - 0.7V - 1.6V}{2k\Omega}\right) = 0.135mA$$

d. The maximum current that the output can sink is

$$I_{OL} = \sigma_{MAX}\beta_F\left[(\beta_R + 1)\left(\frac{V_{CC} - V_{BCA} - 2V_{BES}}{R_B}\right) + \frac{V_{CC} - V_{CES} - V_{BES}}{R_C} - \frac{V_{BES}}{R_D}\right]$$

$$= (0.5)(50)\left[(1.1)\left(\frac{5V - 0.7V - 1.6V}{2k\Omega}\right) + \frac{5V - 0.1V - 0.8V}{3.2k\Omega} - \frac{0.8V}{2k\Omega}\right]$$

$$= 59mA$$

The maximum fan-out based on DC considerations is the largest integer satisfying the inequality

$$N_{MAX} \le \frac{I_{OL}}{I_{IL}} = \frac{59mA}{2.05mA} = 28.8 \text{, or}$$

$$N_{MAX} = 28 .$$

P5.15. For the standard TTL inverter of Figure 5.97 with *scaled resistors*, calculate and plot I_{CCL}, I_{CCH}, I_{IL}, and I_{IH} as functions of x. ¼ < x < 4.

5.19

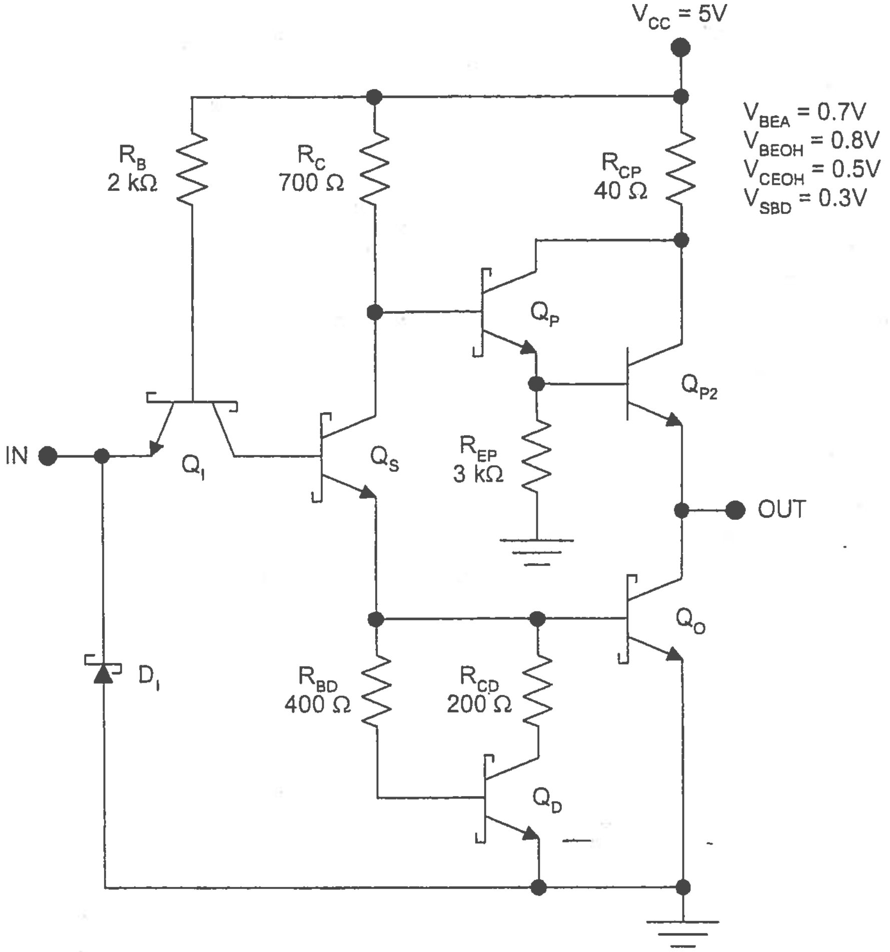

Figure 5.101.

a. Determine V_{IL}, V_{IH}, V_{OL}, and V_{OH}, and plot the voltage transfer characteristic.

b. Determine I_{IL} and I_{IH}.

c. Calculate P_H, P_L, and the average DC power dissipation.

a. The critical voltages are given by

$V_{IL} = 2V_{BEA} - V_{CEOH} = 1.4V - 0.5V = 0.9V$,

$V_{OH} = V_{CC} - 2V_{BEA} = 5V - 1.4V = 3.6V$,

$V_{IH} = 2V_{BEOH} - V_{CEOH} = 1.6V - 0.5V = 1.1V$, and

$V_{OL} = V_{CEOH} = 0.5V$.

The entire voltage transfer characteristic is shown in Figure 5.131.

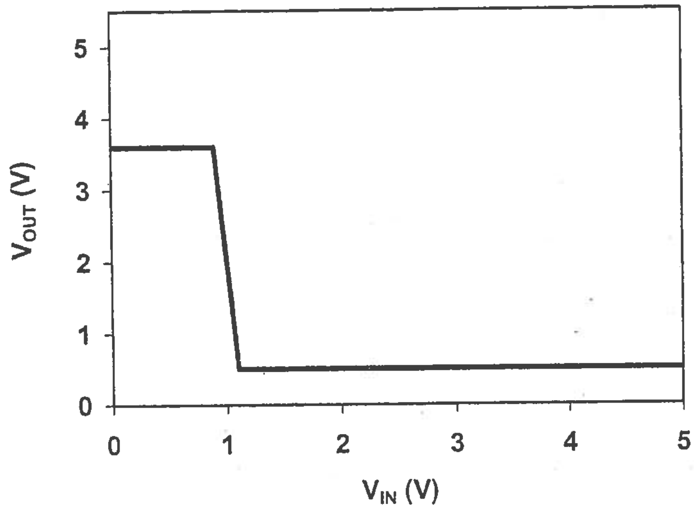

Figure 5.131.

The input low current is

$$I_{IL} = \frac{V_{CC} - V_{BEOH} - V_{CEOH}}{R_B} = \frac{5V - 0.8V - 0.5V}{2k\Omega} = 1.85mA.$$

The input high current is

$I_{IH} \approx 0$.

c. The dissipation is given by

$$P_L = V_{CC}\left(\frac{V_{CC} - V_{SBD} - 2V_{BEOH}}{R_B} + \frac{V_{CC} - V_{CEOH} - V_{BEOH}}{R_C}\right),$$
$$= 5V\left(\frac{5V - 0.3V - 1.6V}{2k\Omega} + \frac{5V - 0.5V - 0.8V}{0.7k\Omega}\right) = 34mW$$

and

$$P_H = V_{CC}\left(\frac{V_{CC} - V_{BEOH} - V_{CEOH}}{R_B}\right) = 5V\left[\frac{5V - 0.8V - 0.5V}{2k\Omega}\right] = 9.2mW.$$

5.21

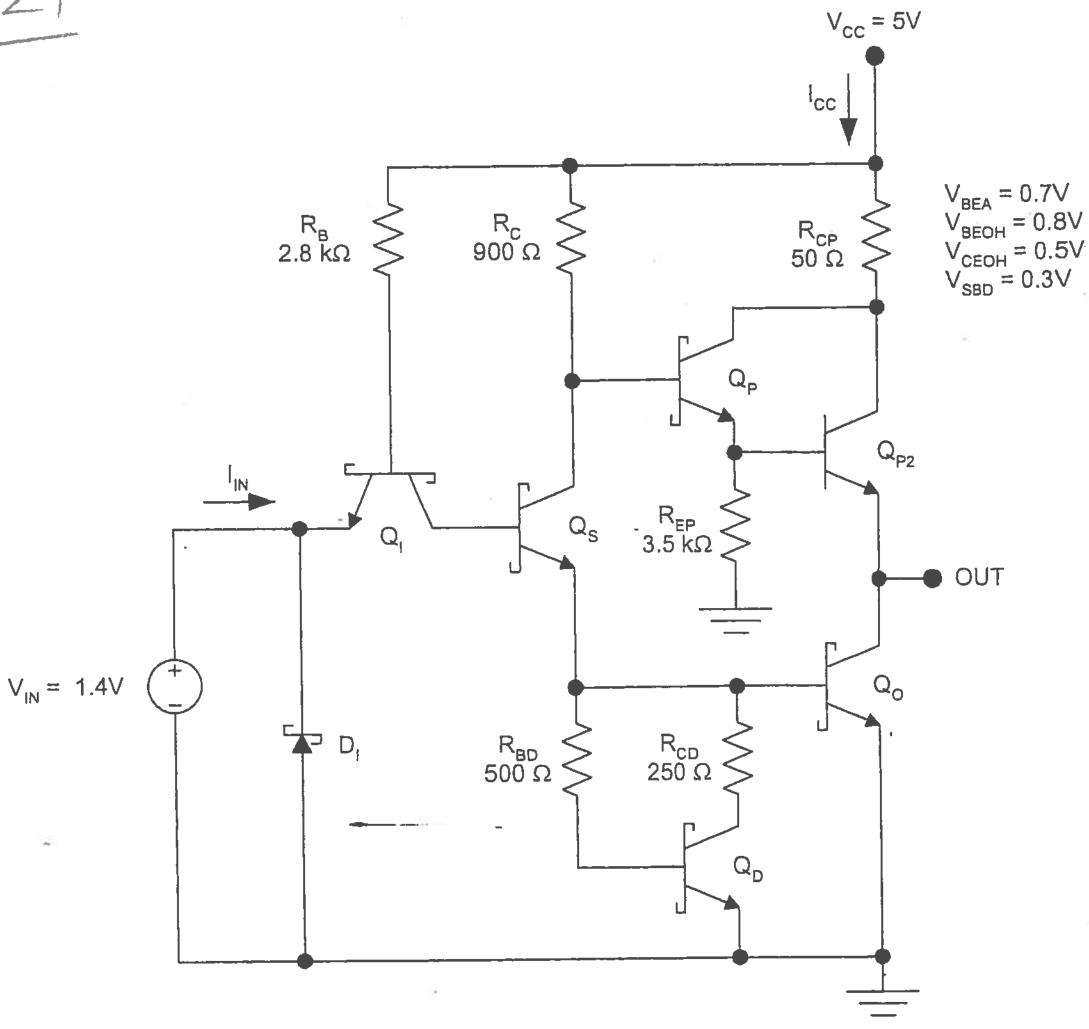

Figure 5.103.

a. Determine the mode of operation for each of the transistors.

b. Determine the value of the input current. Use the convention that the input current is positive if it flows into the emitter of Q_I.

c. Determine the supply current I_{CC}.

d. Determine V_{OUT}.

Solution.

a. Q_I will operate in the reverse Schottky mode. Q_S, Q_O, and Q_D will be on hard. Q_P will be forward active and Q_{P2} will be cutoff.

b. Because Q_I is cutoff,

$$I_{IN} \approx 0 \ .$$

c. The supply current is given by

$$I_{CC} = \frac{V_{CC} - V_{SBD} - 2V_{BEOH}}{R_B} + \frac{V_{CC} - V_{CEOH} - V_{BEOH}}{R_C}$$

$$= \frac{5V - 0.3V - 1.6V}{2.8k\Omega} + \frac{5V - 0.5V - 0.8V}{0.9k\Omega} = 5.2mA$$

d. The output voltage is

$$V_{OUT} = V_{CEOH} = 0.5V \ .$$

P5.22. Consider the inverter shown in Figure 5.104.

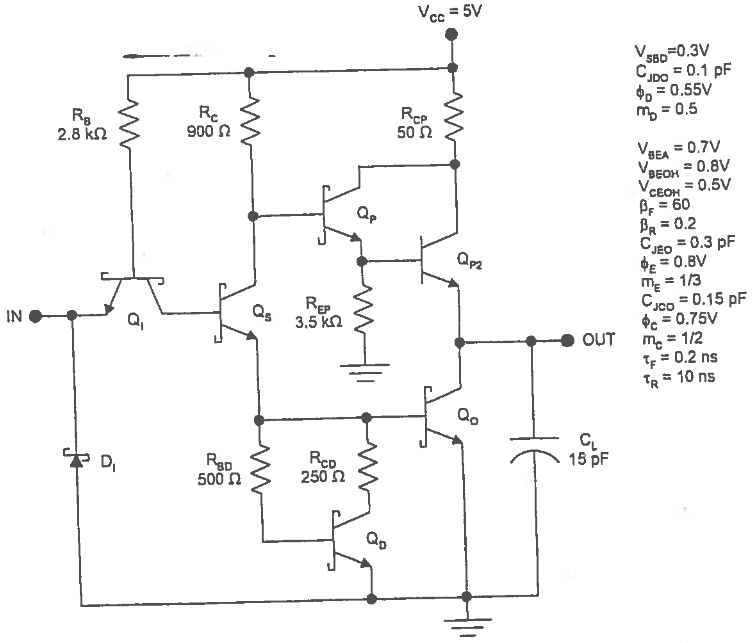

Figure 5.104.

a. Determine t_{PLH} and t_{PHL} for the circuit as shown.