Problem Solutions

Chapter Nine: CMOS Logic

P9.1. Consider the CMOS gate shown in Figure 9.65. $K = 0.2mA/V^2$ and $V_T = 0.6V$.

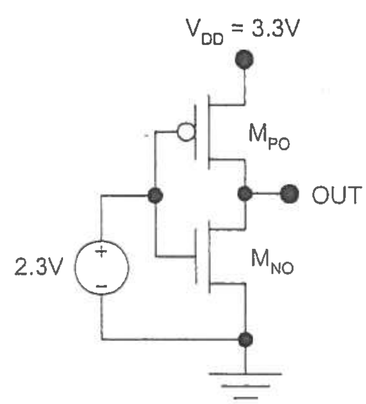

Figure 9.65.

a. Determine the mode of operation for each of the transistors.

b. Determine the supply current I_{DD}.

c. Determine the value of V_{OUT}.

Solution.

a. Because $V_{IN} > V_{DD}/2$, we'll start by assuming that M_{NO} is linear and M_{PO} is saturated. Then, we can determine the supply current by consideration of the saturated transistor:

$$I_{DD} = \frac{0.2mA/V^2(2.3V - 3.3V + 0.6V)^2}{2} = 0.0160mA.$$

The output voltage can be determined by consideration of the linear transistor:

$$V_{OUT} = (2.3V - 06V) - \sqrt{(2.3V - 0.6V)^2 - \frac{2(0.016mA)}{0.2mA/V^2}} = 0.048V$$

Therefore, $V_{GSN} - V_{TN} = 1.7V$ and $V_{DSN} = 0.048V$, consistent with linear operation of M_{NO}. $V_{GSP} - V_{TP} = -0.4V$ and $V_{DSP} = -3.25V$, consistent with saturated operation of M_{PO}.

b. The supply current is

$I_{DD} = 0.0160mA$.

c. The output voltage is

$V_{OUT} = 0.048V$.

P9.2. Consider the CMOS gate shown in Figure 9.66. $K = 0.22mA/V^2$ and $V_T = 0.5V$.

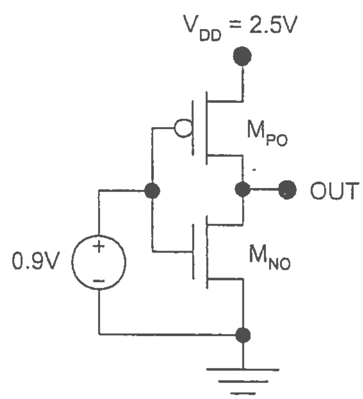

Figure 9.66.

a. Determine the mode of operation for each of the transistors.

b. Determine the supply current I_{DD}.

c. Determine the value of V_{OUT}

Solution.

a. Because $V_{IN} < V_{DD}/2$, we'll start by assuming that M_{NO} is saturated and M_{PO} is linear. Then, we can determine the supply current by consideration of the saturated transistor:

$$I_{DD} = \frac{0.22mA/V^2(0.9V - 0.5V)^2}{2} = 0.0176mA.$$

The output voltage can be determined by consideration of the linear transistor:

$$\begin{aligned} V_{OUT} &= (V_{IN} + V_T) + \sqrt{(V_{IN} - V_{DD} + V_T)^2 - (V_{IN} - V_T)^2} \\ &= (0.9V + 0.5V) + \sqrt{(0.9V - 2.5V + 0.5V)^2 - (0.9V - 0.5V)^2}. \\ &= 2.4V \end{aligned}$$

Therefore, $V_{GSN} - V_{TN} = 0.5V$ and $V_{DSN} = 1.42V$, consistent with saturated operation of M_{NO}. $V_{GSP} - V_{TP} = -1.1V$ and $V_{DSP} = -1.08V$, consistent with linear operation of M_{PO}.

b. $I_{DD} = 0.0176mA$.

c. $V_{OUT} = 2.4V$.

P9.3. Consider the CMOS gate illustrated in Figure 9.67. $K = 0.15mA/V^2$ and $V_T = 0.6V$.

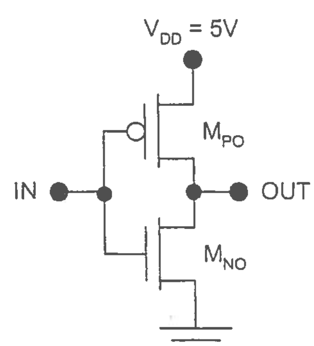

Figure 9.67.

a. Using hand calculations, determine and plot the voltage transfer characteristic for the inverter.

b. Using the results of (a), determine V_{IL}, V_{IH}, V_{OL}, V_{OH}, and the noise margins.

c. Using hand calculations, determine and plot the supply current versus V_{IN} for the inverter.

d. Determine the range of V_{IN} for which the n-MOSFET is linear.

e. Determine the range of V_{IN} for which the p-MOSFET is linear.

f. Using hand calculations, determine and plot the voltage transfer characteristic for the inverter.

Solution.

a. The voltage transfer characteristic can be calculated piecewise as follows.

$$V_{OUT} = \begin{cases} 5V; & V_{IN} \le 0.6V \\ V_{IN} + 0.6V + \sqrt{(V_{IN} - 4.4V)^2 - (V_{IN} - 0.6V)^2}; & 0.6V \le V_{IN} \le 2.5V \\ 2.5V; & V_{IN} = 2.5V \\ V_{IN} - 0.6V - \sqrt{(V_{IN} - 0.6V)^2 - (V_{IN} - 4.4V)^2}; & 2.5V \le V_{IN} \le 4.4V \\ 0; & V_{IN} \ge 4.4V \end{cases}$$

For this example, both transistors are saturated only at $V_{IN} = V_{DD}/2$. Hence, no interpolation is needed. The characteristic is plotted in Figure 9.78. For the symmetric CMOS inverter with matched transistors, the characteristic exhibits odd symmetry about the $V_{DD}/2$ point.

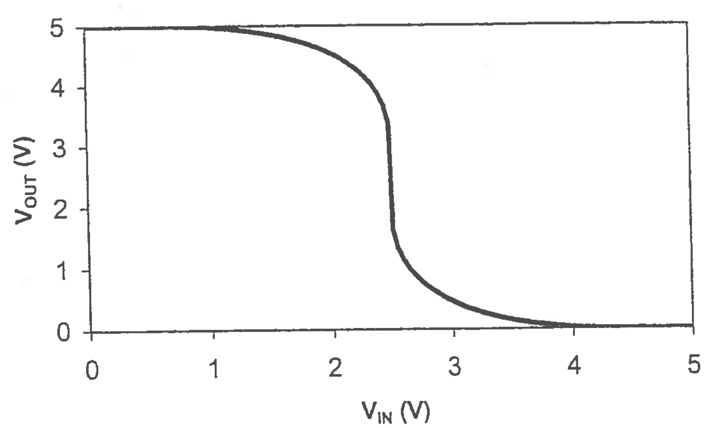

Figure 9.78.

b. From these numerical results, we can determine the critical voltages and the noise margins as follows:

$V_{OL} = 0V$
$V_{IL} = 2.02V$
$V_{IH} = 2.98V$
$V_{OH} = 5V$
$V_{NML} = 2.02V$
$V_{NMH} = 2.02V$

c. The supply current versus the input voltage is given by

$$I_{DD} = \begin{cases} 0; \quad V_{IN} \le 0.6V \\ 75\mu A/V^2 (V_{IN} - 0.6V)^2; \quad 0.6V \le V_{IN} \le 2.5V \\ 75\mu A/V^2 (V_{IN} - 4.4V)^2; \quad 2.5V \le V_{IN} \le 4.4V \\ 0; \quad V_{IN} \ge 4.4V \end{cases}.$$

The results are plotted in Figure 9.79. For the symmetric CMOS inverter with matched transistors, the characteristic is symmetric and the peak current flows when the input voltage is equal to one-half of the supply voltage.

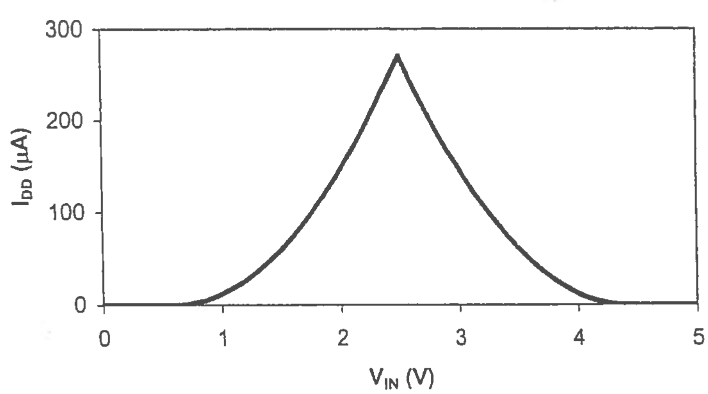

Figure 9.79.

d. The n-MOSFET is linear for $2.5V \le V_{IN} \le 5V$.

e. The p-MOSFET is linear for $0V \le V_{IN} \le 2.5V$.

P9.4. Consider the CMOS gate illustrated in Figure 9.68. $K = 0.15mA/V^2$ and $V_T = 0.45V$.

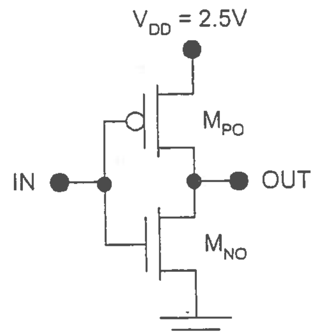

Figure 9.68.

a. Using hand calculations, determine and plot the voltage transfer characteristic for the inverter.

b. Using SPICE, determine and plot the voltage transfer characteristic for the inverter.

c. Using hand calculations, determine and plot the supply current versus V_{IN} for the inverter.

d. Using SPICE, determine and plot the supply current versus V_{IN} for the inverter.

Solution. The voltage transfer characteristic can be calculated piecewise as follows.

$$V_{OUT} = \begin{cases} 2.5V; \quad V_{IN} \le 0.45V \\ V_{IN} + 0.45V + \sqrt{(V_{IN} - 2.05V)^2 - (V_{IN} - 0.45V)^2}; \quad 0.45V \le V_{IN} \le 1.25V \\ 1.25V; \quad V_{IN} = 1.25V \\ V_{IN} - 0.45V - \sqrt{(V_{IN} - 0.45V)^2 - (V_{IN} - 2.05V)^2}; \quad 1.25V \le V_{IN} \le 2.05V \\ 0; \quad V_{IN} \ge 2.05V \end{cases}$$

For this example, both transistors are saturated only at $V_{IN} = V_{DD}/2$. Hence, no interpolation is needed. The characteristic is plotted in Figure 9.80. For the symmetric CMOS inverter with matched transistors, the characteristic exhibits odd symmetry about the $V_{DD}/2$ point.

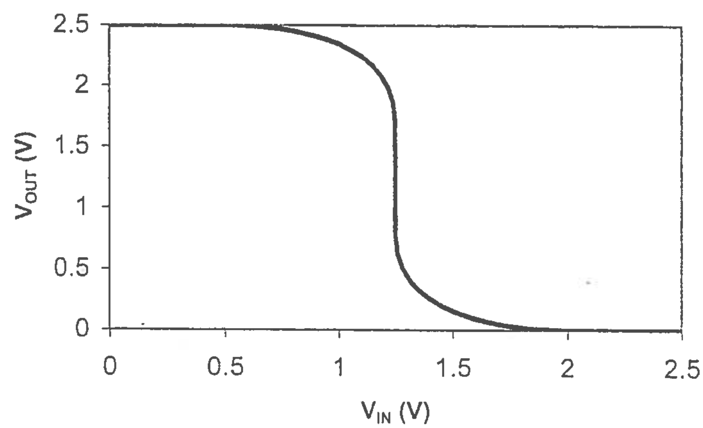

Figure 9.80.

b. The SPICE characteristic is plotted in Figure 9.81.

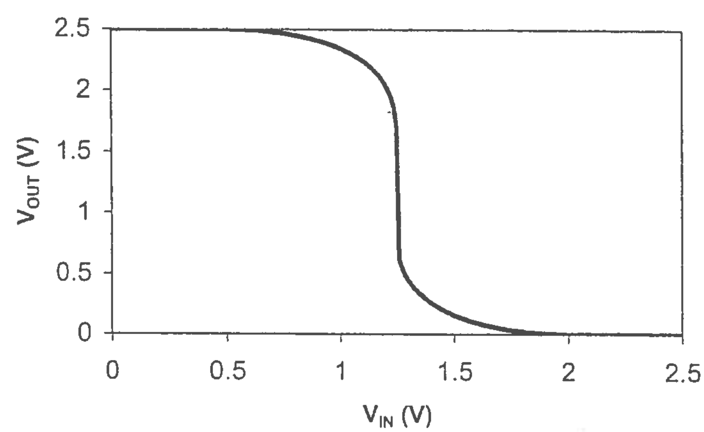

Figure 9.81.

c. The supply current versus the input voltage is given by

$$
I_{DD} = \begin{cases} 0; \quad V_{IN} \le 0.45V \\ 75\mu A/V^2 (V_{IN} - 0.45V)^2; \quad 0.45V \le V_{IN} \le 1.25V \\ 75\mu A/V^2 (V_{IN} - 2.05V)^2; \quad 1.25V \le V_{IN} \le 2.05V \\ 0; \quad V_{IN} \ge 2.05V \end{cases}.
$$

The results are plotted in Figure 9.82. For the symmetric CMOS inverter with matched transistors, the characteristic is symmetric and the peak current flows when the input voltage is equal to one-half of the supply voltage.

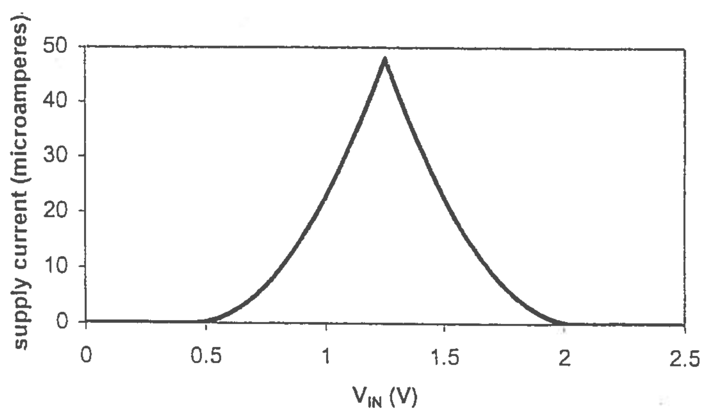

Figure 9.82.

d. The SPICE characteristic is shown in Figure 9.83.

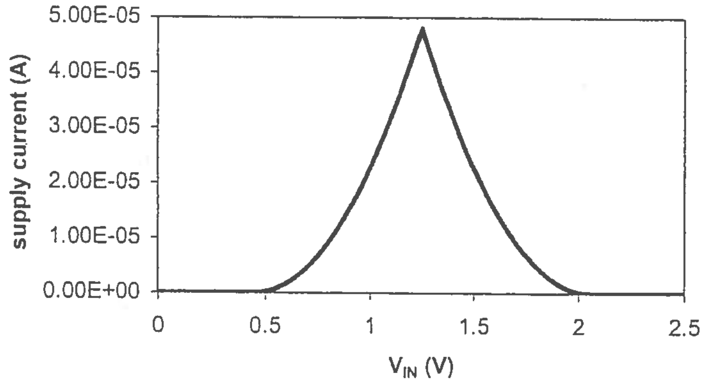

Figure 9.83.

P9.5. Consider the 74HC04 inverter illustrated in Figure 9.69.

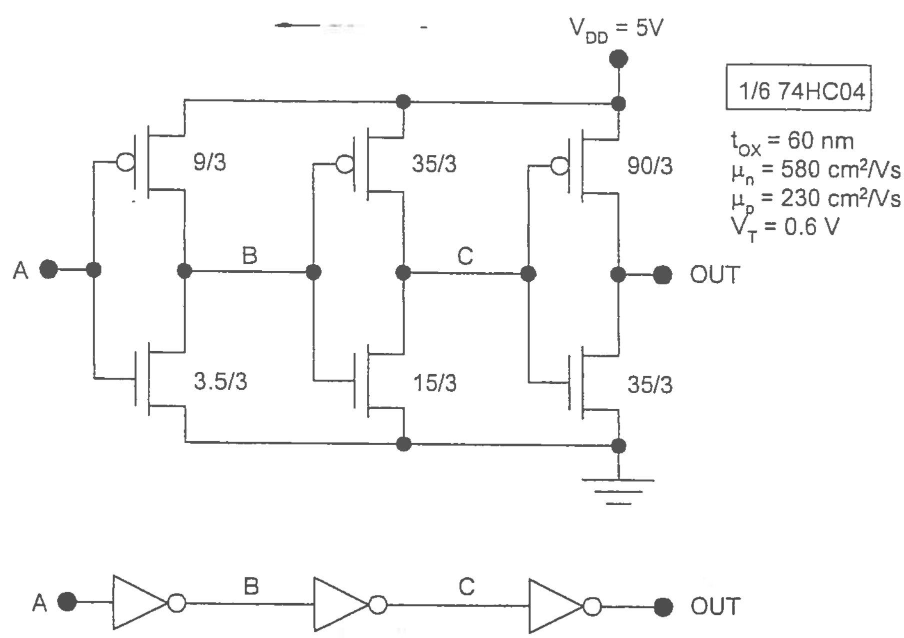

Figure 9.69.

a. Using hand calculations, determine and plot the voltage transfer functions for node B, node C, and the output node.

b. Repeat using SPICE.

Solution.

a. The process transconductance parameters for the p-MOSFETs and n-MOSFETs are

$$k_P' = \frac{\mu_p \varepsilon_{ox}}{t_{ox}} = \frac{(230cm^2/Vs)(3.9)(8.85\times10^{-14}F/cm)}{60\times10^{-7}cm} = 13.4\mu A/V^2$$

and

$$k_N' = \frac{\mu_n \varepsilon_{ox}}{t_{ox}} = \frac{(550cm^2/Vs)(3.9)(8.85\times10^{-14}F/cm)}{60\times10^{-7}cm} = 33.4\mu A/V^2.$$

The voltage transfer characteristic may be calculated using the following three sets of equations:

$$V_B = \begin{cases} 5V; & V_{IN} \le 0.6V \\ V_{IIN} + 0.6V + \sqrt{(V_{IN} - 4.4V)^2 - (V_{IN} - 0.6V)^2}; & 0.6V \le V_{IN} \le 2.5V \\ 2.5V; & V_{IN} = 2.5V \\ V_{IN} - 0.6V - \sqrt{(V_{IN} - 0.6V)^2 - (V_{IN} - 4.4V)^2}; & 2.5V \le V_{IN} \le 4.4V \\ 0; & V_{IN} \ge 4.4V \end{cases}$$

$$V_C = \begin{cases} 5V; & V_B \le 0.6V \\ V_B + 0.6V + \sqrt{(V_B - 4.4V)^2 - (V_B - 0.6V)^2}; & 0.6V \le V_B \le 2.5V \\ 2.5V; & V_B = 2.5V \\ V_B - 0.6V - \sqrt{(V_B - 0.6V)^2 - (V_B - 4.4V)^2}; & 2.5V \le V_B \le 4.4V \\ 0; & V_B \ge 4.4V \end{cases}$$

$$V_{OUT} = \begin{cases} 5V; & V_C \le 0.6V \\ V_C + 0.6V + \sqrt{(V_C - 4.4V)^2 - (V_C - 0.6V)^2}; & 0.6V \le V_C \le 2.5V \\ 2.5V; & V_C = 2.5V \\ V_C - 0.6V - \sqrt{(V_C - 0.6V)^2 - (V_C - 4.4V)^2}; & 2.5V \le V_C \le 4.4V \\ 0; & V_C \ge 4.4V \end{cases}$$

The calculated characteristics are shown in Figure 9.84 as filled squares.

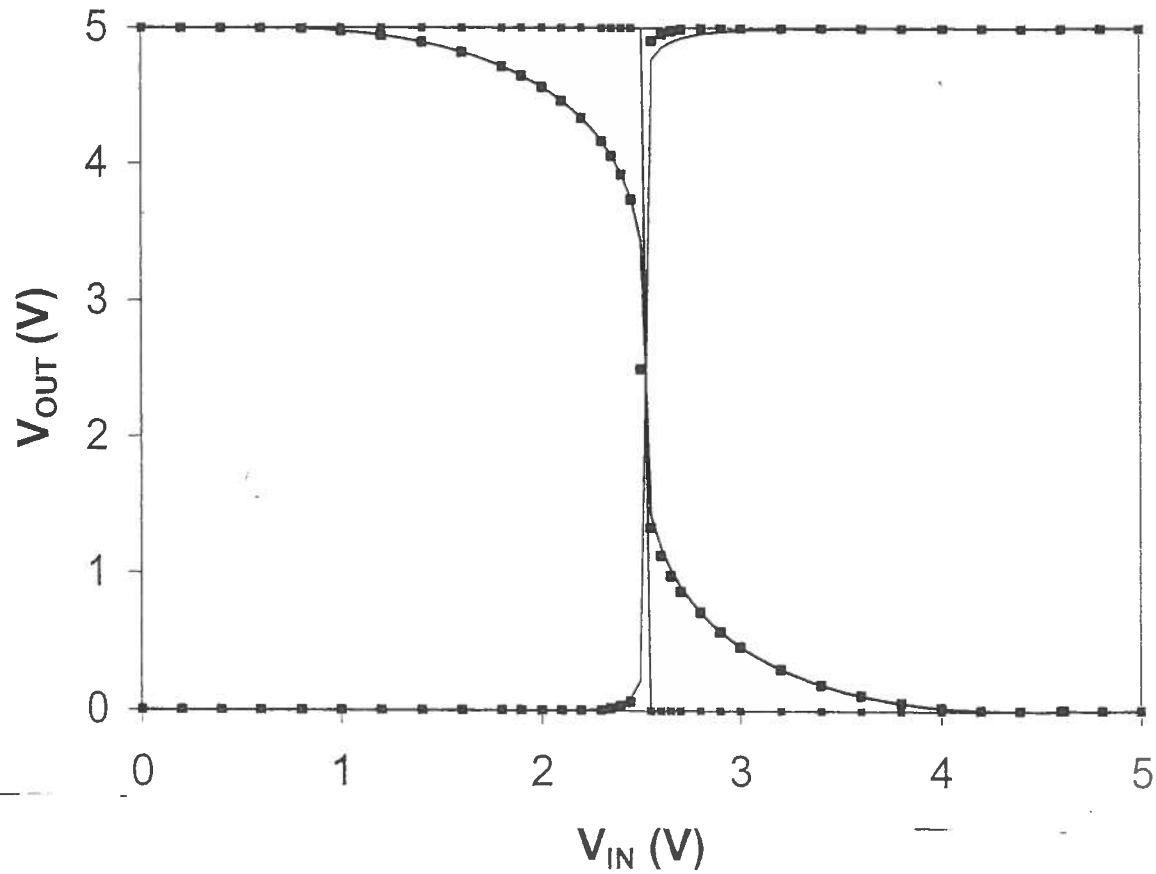

Figure 9.84.

b. The SPICE results are shown in Figure 9.84 as solid curves.

P9.6. Consider the CMOS gate of Figure 9.70.

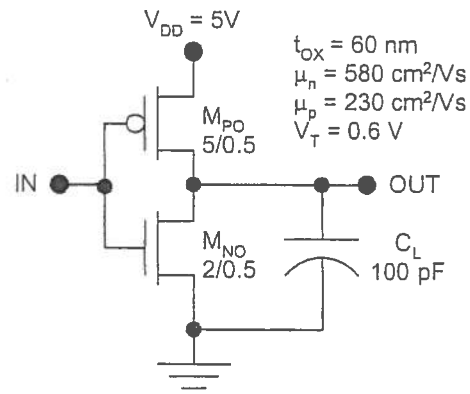

Figure 9.70.

a. Using hand calculations, estimate the propagation delays.

b. Determine the propagation delays using SPICE. Show that t_{PLH} and t_{PHL} are equal, and compare the values to the hand calculation.

Solution.

a. The process transconductance parameters are

$$k_P' = \frac{(230cm^2/Vs)(3.9)(8.85\times10^{-14}F/cm)}{600\times10^{-8}cm} = 0.0133mA/V^2$$

and

$$k_N' = \frac{(580cm^2/Vs)(3.9)(8.85\times10^{-14}F/cm)}{600\times10^{-8}cm} = 0.033mA/V^2.$$

The device transconductance parameters are

$$K_P = \left(\frac{5}{0.5}\right)0.0133mA/V^2 = 0.133mA/V^2$$

and

$$K_N = \left(\frac{2}{0.5}\right)0.033mA/V^2 = 0.132mA/V^2.$$

The propagation delays will be approximately

$$t_P \approx \frac{100\times10^{-15}F}{0.132\times10^{-3}A/V^2}\left[\frac{1.2V}{(4.4V)^2}+\frac{2}{4.4V}\ln\left(\frac{4.4V}{2.5V}\right)\right]=240ns.$$

b. From the SPICE results, $t_{PLH} = t_{PHL} = 200ns$ as shown in Figure 9.85.

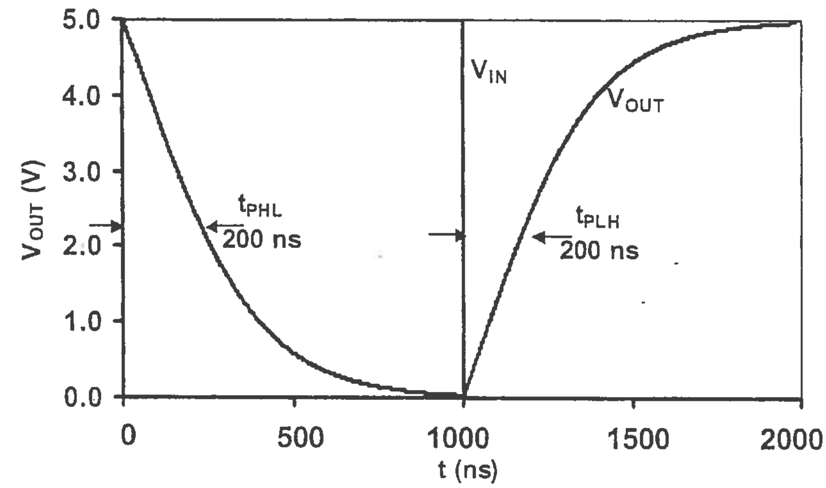

Figure 9.85.

P9.7. For the CMOS gate shown in Figure 9.71, estimate the maximum fan-out if $t_{P,MAX} = 300ps$.

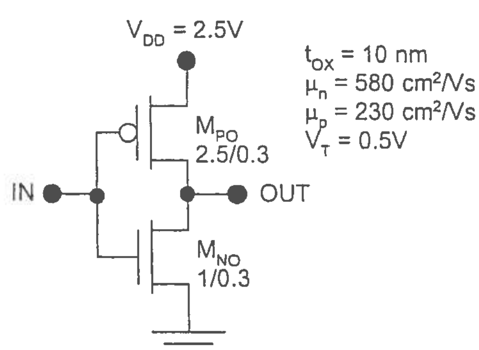

Figure 9.71.

Solution. The input capacitance for the gate is

$$C_{IN} = C_{OXN} + C_{OXP} = \frac{\varepsilon_{OX} W_N L_N}{t_{OX}} + \frac{\varepsilon_{OX} W_P L_P}{t_{OX}}$$

$$= \frac{(3.9)(8.85\times10^{-14}\,F/cm)[(0.3\times10^{-4}\,cm)(2.5\times10^{-4}\,cm)+(0.3\times10^{-4}\,cm)(1\times10^{-4}\,cm)]}{100\times10^{-8}\,cm}.$$

$$= 3.6\,fF$$

The transconductance parameters may be determined as follows:

$$k_P' = \frac{(230cm^2/Vs)(3.9)(8.85\times10^{-14}\,F/cm)}{100\times10^{-8}\,cm} = 0.080mA/V^2,$$

$$k_N' = \frac{(580cm^2/Vs)(3.9)(8.85\times10^{-14}\,F/cm)}{100\times10^{-8}\,cm} = 0.20mA/V^2,$$

$$K_P = \left(\frac{2.5}{0.3}\right)0.080mA/V^2 = 0.67mA/V^2, \text{ and}$$

$$K_N = \left(\frac{1}{0.3}\right)0.20mA/V^2 = 0.67mA/V^2.$$

The maximum load capacitance is

$$C_{L,\max} \approx \frac{Kt_{P,\max}}{\left[\frac{2V_T}{(V_{DD}-V_T)^2} + \frac{2}{(V_{DD}-V_T)}\ln\left(\frac{V_{DD}-V_T}{V_{DD}/2}\right)\right]}.$$

$$= \frac{(0.67\times10^{-3}\,A/V^2)(300\times10^{-12}\,s)}{\left[\frac{1.0V}{(2.0V)^2} + \frac{2}{2.0V}\ln\left(\frac{2.0V}{1.25V}\right)\right]} = 2.8\times10^{-13}\,F$$

The maximum fan-out is therefore given by

$$N_{MAX} \le \frac{C_{L,\max}}{C_{IN}} = \frac{2.8\times10^{-13}\,F}{3.6\times10^{-15}\,F} = 78, \text{ or}$$

$$N_{MAX} = 78.$$

P9.8. For the CMOS gate of Figure 9.72, estimate the maximum fan-out if the clock frequency is to be 100 MHz.

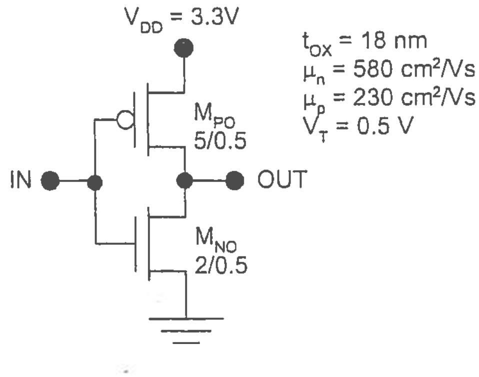

Figure 9.72.

Solution. The input capacitance for the gate is

$$C_{IN} = C_{OXN} + C_{OXP} = \frac{\varepsilon_{OX} W_N L_N}{t_{OX}} + \frac{\varepsilon_{OX} W_P L_P}{t_{OX}}$$

$$= \frac{(3.9)(8.85\times10^{-14}\,F/cm)\left[(0.5\times10^{-4}\,cm)(2\times10^{-4}\,cm)+(0.5\times10^{-4}\,cm)(5\times10^{-4}\,cm)\right]}{18\times10^{-7}\,cm}$$

$$= 6.7\,fF$$

The transconductance parameters may be determined as follows:

$$k_P' = \frac{(230cm^2/Vs)(3.9)(8.85\times10^{-14}\,F/cm)}{18\times10^{-7}\,cm} = 0.044mA/V^2,$$

$$k_N' = \frac{(580cm^2/Vs)(3.9)(8.85\times10^{-14}\,F/cm)}{18\times10^{-7}\,cm} = 0.111mA/V^2,$$

$$K_P = \left(\frac{5}{0.5}\right)0.044mA/V^2 = 0.44mA/V^2, \text{ and}$$

$$K_N = \left(\frac{2}{0.5}\right)0.111mA/V^2 = 0.44mA/V^2.$$

The maximum allowable propagation delay is approximately

$$t_{P,\max} = \frac{1}{20 f_{CLK}} = 0.5ns .$$

The maximum load capacitance is

$$C_{L,\max} \approx \frac{Kt_{P,\max}}{\left[\frac{2V_T}{(V_{DD}-V_T)^2} + \frac{2}{(V_{DD}-V_T)}\ln\left(\frac{V_{DD}-V_T}{V_{DD}/2}\right)\right]}.$$

$$= \frac{(0.44\times10^{-3}\,A/V^2)(0.5\times10^{-9}\,s)}{\left[\frac{1.0V}{(2.8V)^2} + \frac{2}{2.8V}\ln\left(\frac{2.8V}{1.65V}\right)\right]}$$

$$= 4.3\times10^{-13}\,F$$

The maximum fan-out is therefore given by

$$N_{MAX} \le \frac{C_{L,\max}}{C_{IN}} = \frac{4.3\times10^{-13}\,F}{6.7\times10^{-15}\,F} = 64, \text{ or}$$

$$N_{MAX} = 64.$$

P9.9. Consider CMOS circuitry driving a 50 pF off-chip load as shown in Figure 9.73. $t_{ox} = 16$ nm. $V_T = 0.5V$. Suppose that each successive stage is scaled up in current driving capability by a factor of 3.

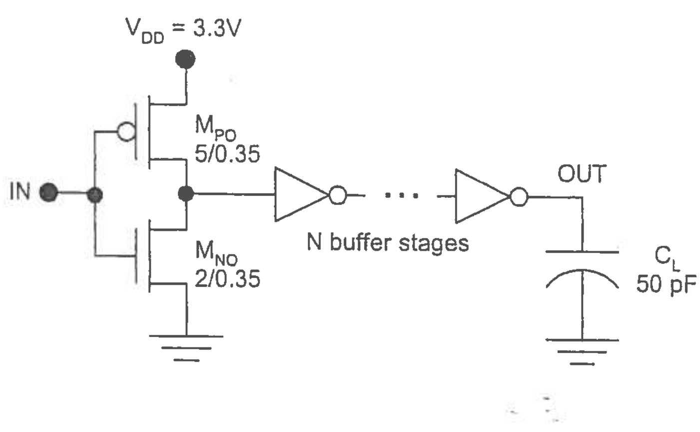

Figure 9.73.

a. Determine the required number of buffer stages such that $t_P \le 0.6$ ns.

b. Use SPICE to verify your design.

Solution.

a. For each stage,

$$t_P = \frac{C_L}{K}\left[\frac{2V_T}{(V_{DD}-V_T)^2} + \frac{2}{(V_{DD}-V_T)}\ln\left(\frac{V_{DD}-V_T}{V_{DD}/2}\right)\right] = \frac{C_L}{K}\left[0.505V^{-1}\right].$$

The process transconductance parameters are:

$$k_P' = \frac{(230cm^2/Vs)(3.9)(8.85\times10^{-14}F/cm)}{160\times10^{-8}cm} = 50\mu A/V^2$$

and

$$k_N' = \frac{(580cm^2/Vs)(3.9)(8.85\times10^{-14}F/cm)}{160\times10^{-8}cm} = 125\mu A/V^2.$$

The input capacitance for any stage is proportional to the K value:

$$C_{IN} = \frac{5.3fF}{0.71mA/V^2}K_N.$$

With no buffers,

$$t_P = \frac{50pF}{0.71mA/V^2}\left[0.505V^{-1}\right] = 36ns.$$

If the scale factor is constrained to be three, then four buffers are required because

$$3^3 < \frac{36ns}{0.6ns} < 3^4.$$

b. The SPICE simulation results of Figure 9.86 show that the propagation delays are 0.38ns with four buffers.

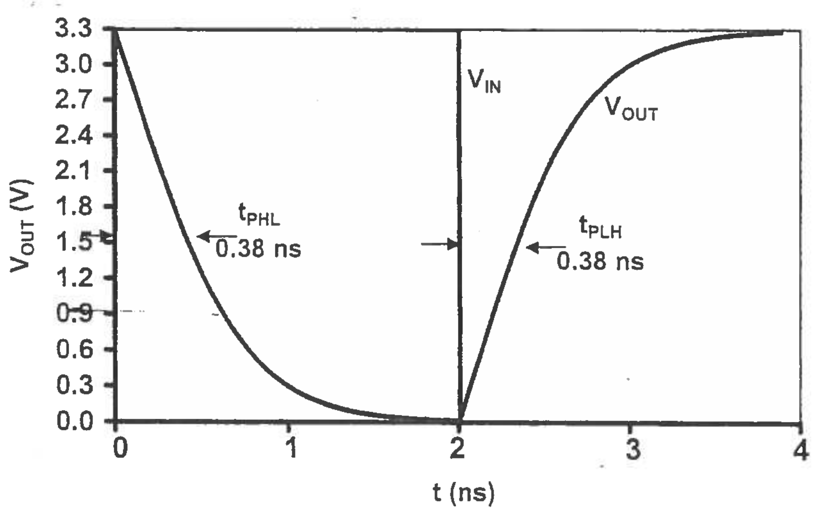

Figure 9.86.

P9.10. Consider CMOS circuitry driving a 50 pF off-chip load as illustrated in Figure 9.74. t_{ox} = 11 nm. V_T = 0.5V.

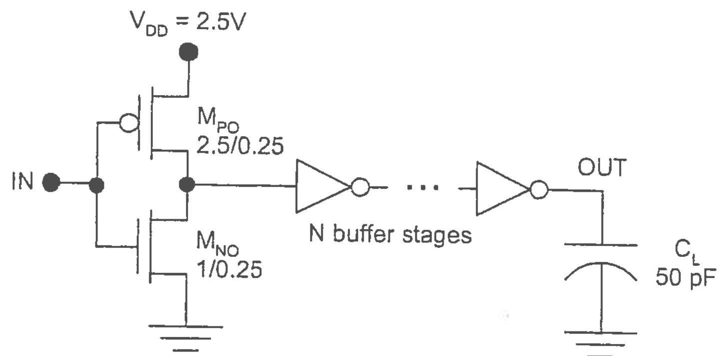

Figure 9.74.

a. Determine the minimum number of buffer stages necessary such that $t_P < 1$ ns.

b. For each buffer stage, determine the required gate dimensions for each of the MOSFETs.

c. Use SPICE to verify your design.

Solution.

a. For each stage

$$t_P = \frac{C_L}{K}\left[\frac{2V_T}{(V_{DD}-V_T)^2} + \frac{2}{(V_{DD}-V_T)}\ln\left(\frac{V_{DD}-V_T}{V_{DD}/2}\right)\right] = \frac{C_L}{K}\left[0.72V^{-1}\right]$$

The process transconductance parameters are:

$$k_P' = \frac{(230cm^2/Vs)(3.9)(8.85\times10^{-14}F/cm)}{110\times10^{-8}cm} = 72\mu A/V^2$$

$$k_N' = \frac{(580cm^2/Vs)(3.9)(8.85\times10^{-14}F/cm)}{110\times10^{-8}cm} = 182\mu A/V^2$$

The input capacitance for any stage is proportional to the K value:

$$C_{IN} = \frac{2.75fF}{0.728mA/V^2}K_N$$

With no buffers,

$$t_P = \frac{50pF}{0.73mA/V^2}\left[0.72V^{-1}\right] = 49ns$$

Therefore, some buffering is necessary. With one buffer, suppose the delay for the last stage is 1ns/2. Then

$$K_0 = 0.73mA/V^2 \quad t_{P0} = 0.27ns$$
$$K_1 = 72mA/V^2 \quad C_{IN1} = 272fF \quad t_{P1} = 0.5ns$$
$$t_P = 0.77ns$$

Therefore one buffer is sufficient.

b. For the buffer stage,

$$K_N = K_P = 72mA/V^2$$

so that

$$W_p = 0.25\mu m\left(\frac{72mA/V^2}{0.072\mu A/V^2}\right) = 250\mu m$$

and

$$W_N = 0.25\mu m\left(\frac{72mA/V^2}{0.182\mu A/V^2}\right) = 99\mu m\ .$$

b. The SPICE transient results show that the propagation delays are both 0.8ns.

P9.11. For the CMOS gate shown in Figure 9.75, perform an analysis of constant voltage scaling. (Assume that the oxide thickness and all gate dimensions are scaled by 1/s). $1 \le s \le 10$.

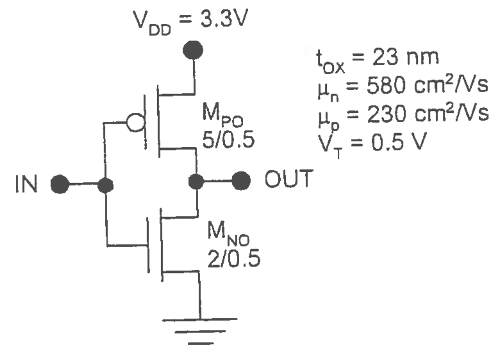

Figure 9.75.

a. Determine and plot the propagation delay versus s, assuming 20 on-chip loads.

b. Determine and plot the dissipation versus s, assuming 20 on-chip loads and $f = 0.05/t_P$.

Solution.

a. The process transconductance parameters are

$$k_P' = \frac{(230cm^2/Vs)(3.9)(8.85\times10^{-14}F/cm)}{23\times10^{-7}cm} = 0.034mA/V^2$$

and

$$k_N' = \frac{(580cm^2/Vs)(3.9)(8.85\times10^{-14}F/cm)}{23\times10^{-7}cm} = 0.087mA/V^2.$$

With s = 1,

$$C_{IN} = C_{OXN} + C_{OXP} = \frac{\varepsilon_{OX}W_N L_N}{t_{OX}} + \frac{\varepsilon_{OX}W_P L_P}{t_{OX}}$$

$$= \frac{(3.9)(8.85\times10^{-14}F/cm)[(2\times10^{-4}cm)(0.5\times10^{-4}cm)+(5\times10^{-4}cm)(0.5\times10^{-4}cm)]}{23\times10^{-7}cm},$$

$$= 5.2fF$$

$$K_P = \left(\frac{5}{0.5}\right)0.034mA/V^2 = 0.34mA/V^2,$$

$$K_N = \left(\frac{2}{0.5}\right)0.087mA/V^2 = 0.35mA/V^2,$$

and

$$t_P \approx \frac{20\left(5.2\times10^{-15}F\right)}{0.34\times10^{-3}A/V^2}\left[\frac{1.0V}{(2.8V)^2}+\frac{2}{2.8V}\ln\left(\frac{2.8V}{1.65V}\right)\right] = 0.155ns.$$

Using constant-voltage scaling,

$$t_P = \frac{0.155ns}{s^2}.$$

This is plotted in Figure 9.87.

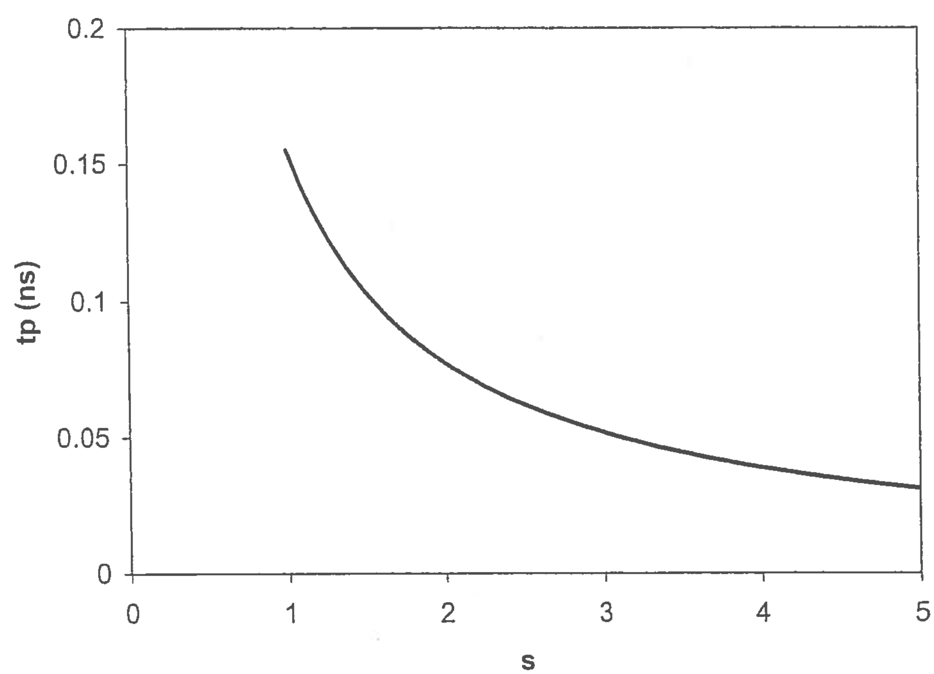

Figure 9.87.

b. The dissipation may be determined as a function of s, assuming 20 on-chip loads and f = $0.05/t_P$, as follows:

$$C_{IN} = \frac{5.2fF}{s},$$

$$C_L = 20C_{IN} = \frac{104fF}{s},$$

$$f = \frac{0.05s}{0.155ns},$$

and

$$P = fC_L V_{DD}^2 = \left(\frac{0.05s}{0.155ns}\right)\left(\frac{104fF}{s}\right)(3.3V)^2 = 0.365mW.$$

The dissipation is independent of s if it is assumed that the clock frequency scales inversely with the propagation delay.

P9.12. For the CMOS gate of Figure 9.76, perform an analysis of "full" scaling. (Assume that the oxide thickness, all gate dimensions, and V_{DD} are scaled by 1/s.) $1 \le s \le 5$.

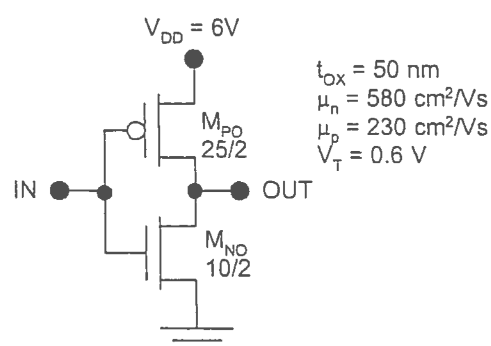

Figure 9.76.

a. Determine and plot the propagation delay versus s, assuming 20 on-chip loads.

b. Determine and plot the dissipation versus s, assuming 20 on-chip loads and f = 0.05/t_P.

Solution. The process transconductance parameters are

$$k_P' = \frac{(230cm^2/Vs)(3.9)(8.85\times10^{-14}F/cm)}{50\times10^{-7}cm} = 0.016mA/V^2$$

and

$$k_N' = \frac{(580cm^2/Vs)(3.9)(8.85\times10^{-14}F/cm)}{50\times10^{-7}cm} = 0.040mA/V^2.$$

With s = 1,

$$C_{IN} = C_{OXN} + C_{OXP} = \frac{\varepsilon_{OX}W_N L_N}{t_{OX}} + \frac{\varepsilon_{OX}W_P L_P}{t_{OX}}$$
$$= \frac{(3.9)(8.85\times10^{-14}F/cm)[(10\times10^{-4}cm)(2\times10^{-4}cm)+(25\times10^{-4}cm)(2\times10^{-4}cm)]}{50\times10^{-7}cm},$$
$$= 48fF$$

$$K_P = \left(\frac{25}{2}\right)0.016mA/V^2 = 0.20mA/V^2,$$

$$K_N = \left(\frac{10}{2}\right)0.040mA/V^2 = 0.2mA/V^2,$$

and

$$t_P \approx \frac{20(48\times10^{-15}F)}{0.2\times10^{-3}A/V^2}\left[\frac{1.2V}{(5.4V)^2} + \frac{2}{5.4V}\ln\left(\frac{5.4V}{3V}\right)\right] = 1.24ns.$$

Using full scaling,

$$t_P = \frac{1.24ns}{s}.$$

This is plotted in Figure 9.88.

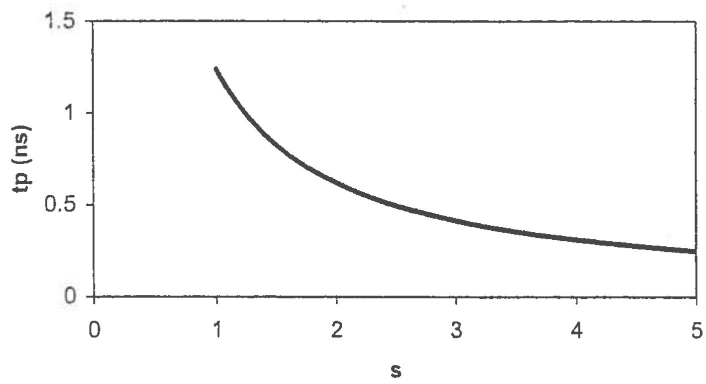

Figure 9.88.

b. The dissipation may be determined as a function of s, assuming 20 on-chip loads and f = $0.05/t_P$, as follows:

$$C_{IN} = \frac{48\,fF}{s},$$

$$C_L = 20C_{IN} = \frac{960\,fF}{s},$$

$$f = \frac{0.05s}{1.24ns},$$

$$V_{DD} = \frac{6V}{s},$$

and

$$P = fC_L V_{DD}^2 = \left(\frac{0.05s}{1.24ns}\right)\left(\frac{960\,fF}{s}\right)\left(\frac{6V}{s}\right)^2 = \frac{1.39mW}{s^2}.$$

The results are plotted in Figure 9.89.

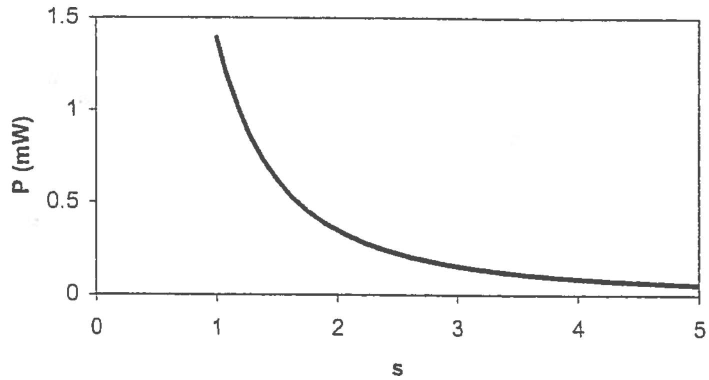

Figure 9.89.

P9.13. The gate shown in Figure 9.77 represents 1975 technology. Assume that constant voltage scaling is used, with a scale factor of $1/\sqrt{2}$ applied every eighteen months. Estimate and plot the microprocessor clock frequency versus the year, up to the present time. Assume N = 20.

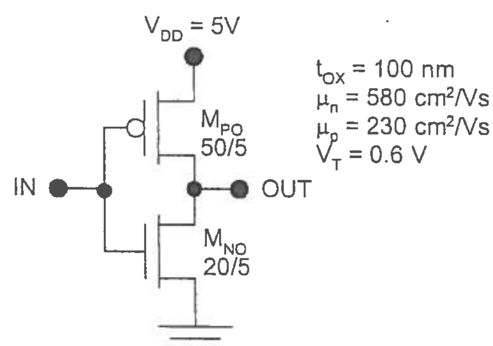

Figure 9.77.

Solution. The process transconductance parameters are given by

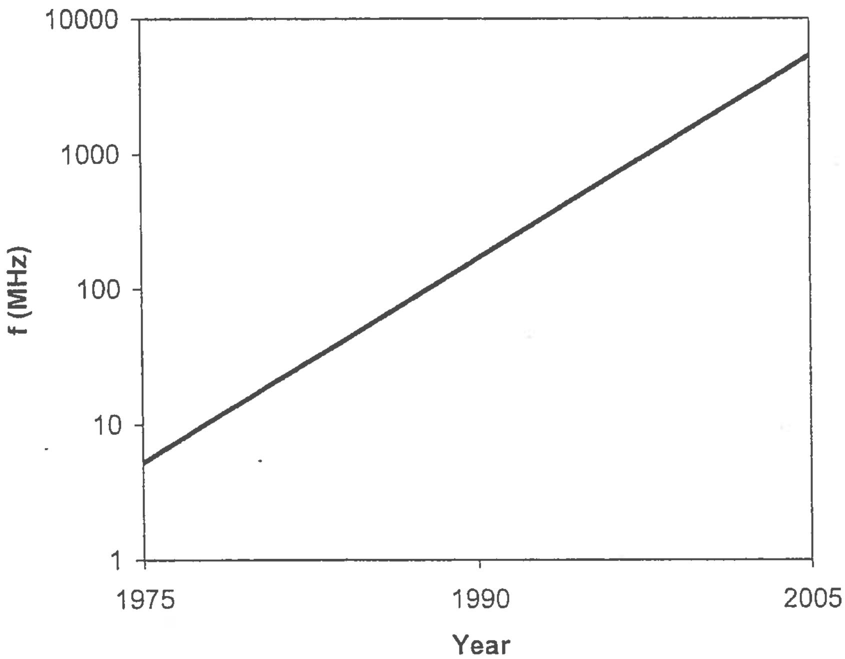

Figure 9.90.

$$K_O \geq \frac{0.44nsA/V^2}{10ns} = 44mA/V^2 .$$

From the dissipation requirement,

$$P_{DC} = \frac{K_L V_{DD} V_{TL}^2}{4} = \frac{K_L (3.3V)(-0.3V)^2}{4} \leq 1mW$$

or

$$K_L \leq 13.5mA/V^2 .$$

It is not possible to satisfy all three requirements.